EXHIBIT C

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WOLFSPEED, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY.
Patent Owner

U.S. Patent No. 7,498,633
Inter Partes Review No. 2022-00761

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,498,633 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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EXHIBIT LIST

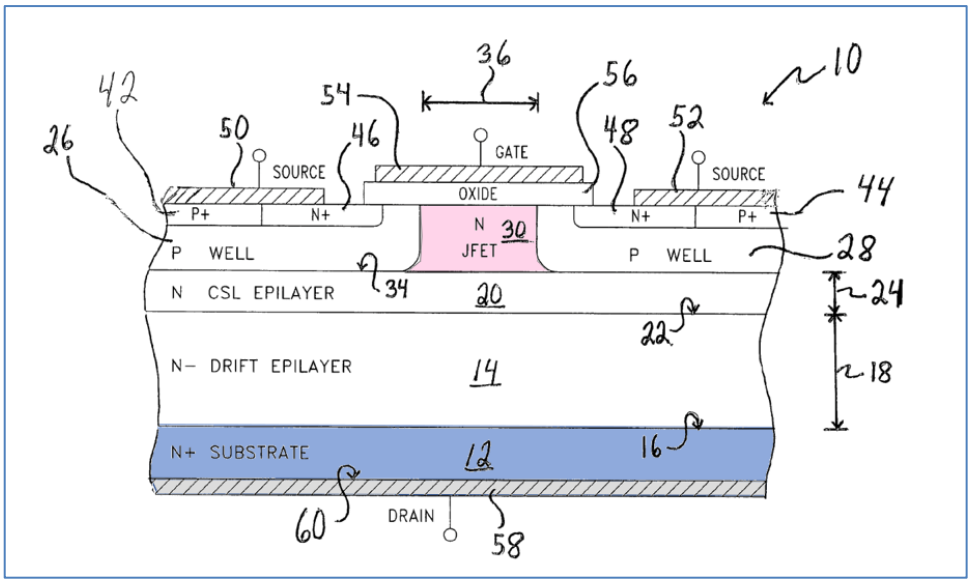
No.	Short Name	Exhibit
1001	'633 Patent	U.S. Patent No. 7,498,633 to Cooper and Saha
1002	'633 Prosecution History	Prosecution history for U.S. Patent No. 7,498,633
1003	Ryu	U.S. Patent Pub. No. 2004/0119076 to Ryu
1004	Depetro	U.S. Patent No. 6,043,532 to Depetro
1005	Choy	U.S. Patent No. 5,171,705 to Choy
1006	Williams	U.S. Patent No. 6,413,822 to Williams
1007	Nakayama	U.S. Patent Pub. No. 2004/0046202 to Nakayama
1008	Baliga	Baliga, *Modern Power Devices*, Wiley (1987)
1009	Hu	Hu, *Optimum Design of Power MOSFETs*, IEEE Transactions on Electron Devices, Ed-31, No. 12 (1984)
1010	Lee Declaration	Declaration of Dr. Jack Lee, Ph.D.
1011	Grant	Grant & Gowar, *Power MOSFETs, Theory and Applications*, Wiley (1989)
1012	Ghezzo	U.S. Patent No. 5,510,281 to Ghezzo et al.
1013	Baliga Patent	U.S. Patent No. 5,233,215 to Baliga
1014	Knoch	U.S. Patent No. 5,703,389 to Knoch et al.
1015	Ryu Paper	Ryu et al., *Design and Process Issues for Silicon Carbide Power DiMOSFETS*, Mat. Res. Soc. Symp. Vol. 640 (2001)

No.	Short Name	Exhibit
1016	Wolfspeed Complaint	Complaint from *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 21-cv-00840 (M.D.N.C.)
1017	STM Complaint	Complaint from *The Trustees of Purdue University v. STMicroelectronics NV et al.*, No. 21-cv-00727 (W.D.T.X.)
1018	'152 Application	U.S. Provisional Application No. 60/646,152
1019	Barkhordarian	Barkhordarian, *Power MOSFET Basics*, International Rectifier
1020	A&O	Power MOSFET Basics, Alpha & Omega
1021	Suvorov	U.S. Patent No. 6,107,142 to Suvorov et al.
1022	Suvorov-2	U.S. Patent No. 6,100,169, also to Suvorov et al.
1023	Palmour	U.S. Patent No. 5,506,421 to Palmour

I. INTRODUCTION

Petitioner Wolfspeed, Inc. ("Wolfspeed") requests that the Board institute *inter partes* review ("IPR") and cancel claims 9-11 of U.S. Patent No. 7,498,633 (the "'633 Patent"), assigned to Patent Owner The Trustees of the University of Purdue ("Purdue").

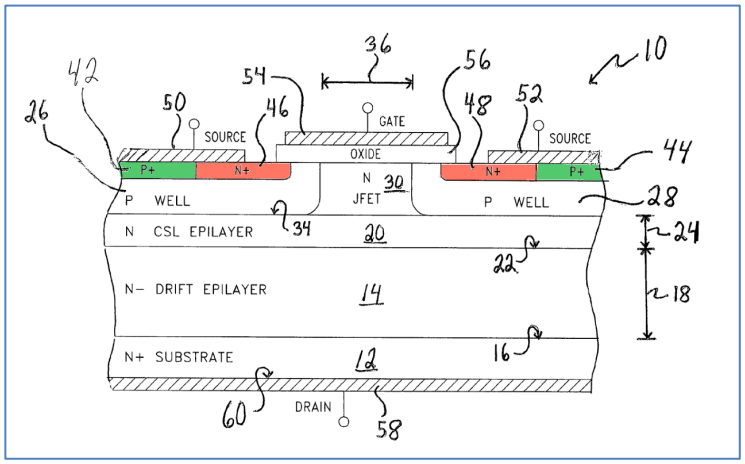
The challenged claims are directed to a silicon-carbide ("SiC") metal-oxide-semiconductor field-effect transistor ("MOSFET"). During prosecution, the Applicant relied on a single feature of the claimed MOSFET to distinguish it over the prior art: a junction-field-effect transistor ("JFET") region formed on a SiC substrate. The JFET region (pink) and SiC substrate (blue) are illustrated in the cross section below:



Ex. 1001 at Fig. 1.[1]

[1] Images with color have been annotated unless otherwise noted.

According to the Applicant, it would not have been obvious to incorporate the claimed JFET region onto a SiC substrate. The Examiner disagreed and found both features present in the prior art and obvious to combine to achieve known benefits. The Examiner ultimately allowed the claims, but only because they described a source-region layout comprising spaced-apart base-contact regions. The source region (red) and base-contact regions (green) are shown in the cross-section and overhead images below:



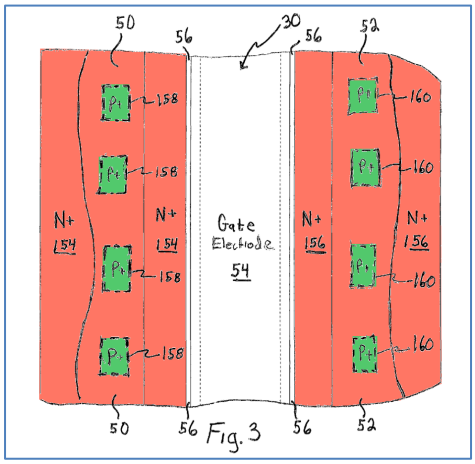


Fig. 3

Id. at Figs. 1, 3.

Although the Applicant never relied on the source-region layout as a point of novelty, the Examiner concluded that the feature was missing from the prior art. The Examiner, however, did not have the benefit of the references cited in this Petition. Those references demonstrate that the claimed source-region layout was a common MOSFET design which had been incorporated into both silicon and SiC devices as shown below:

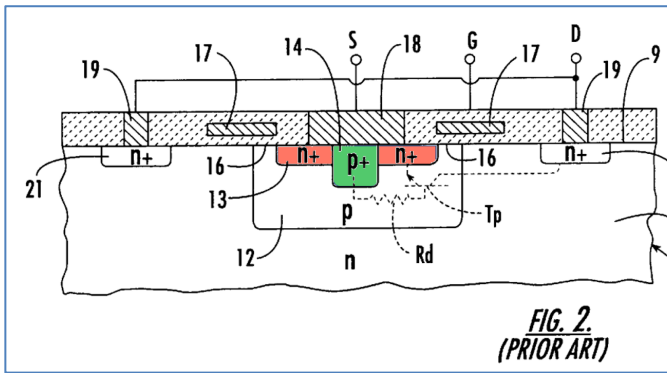


FIG. 2.
(PRIOR ART)

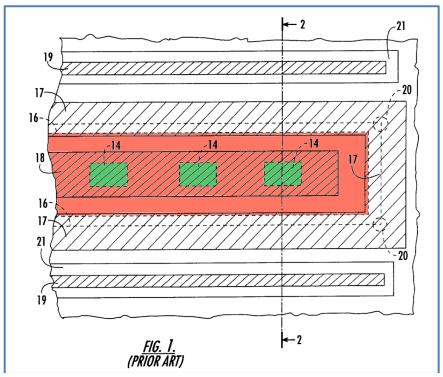


FIG. 1.
(PRIOR ART)

Ex. 1004 ("Depetro") at Figs. 1-2.

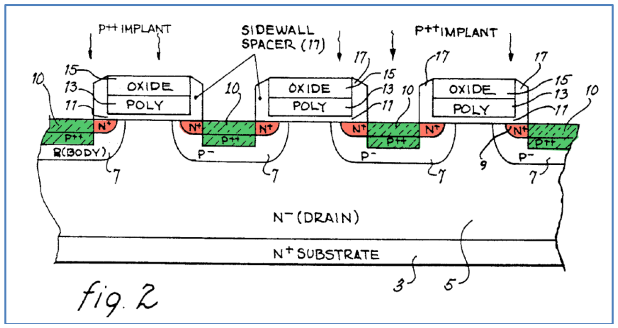


fig. 2

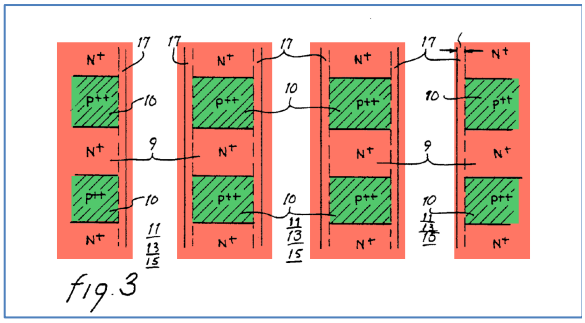
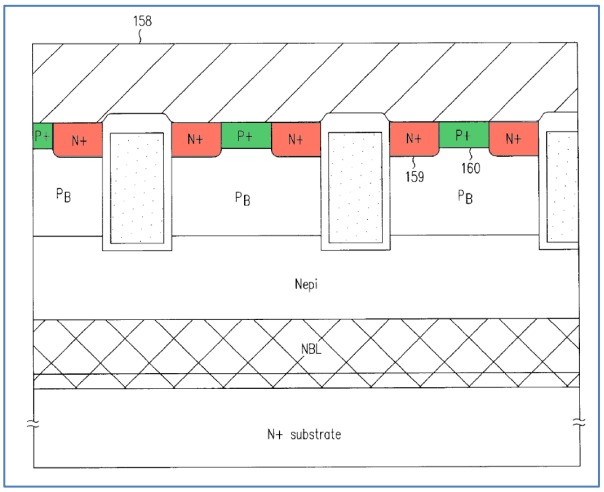
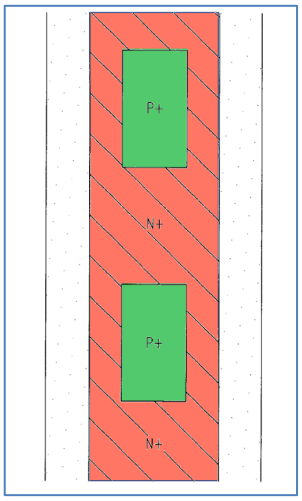


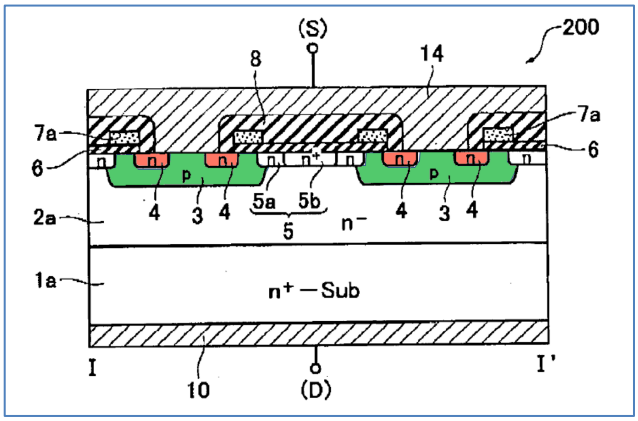
fig. 3

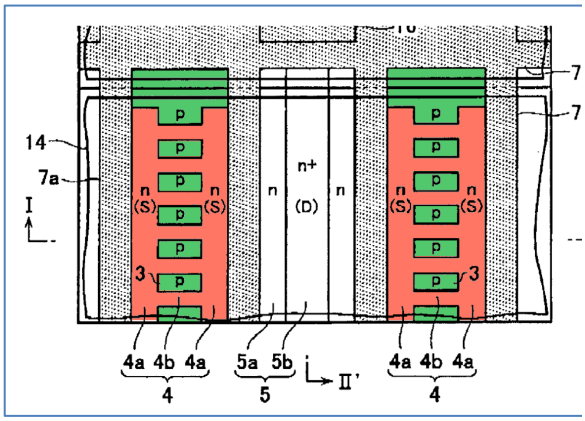
Ex. 1005 ("Choy") at Figs. 2-3.





Ex. 1006 ("Williams") at Figs. 1, 19E.





Ex. 1007 ("Nakayama") at Figs. 9, 11.

The above references not only teach the structure of the claimed source region layout, but also the known benefit of incorporating it into a MOSFET: to reduce on-resistance, a key performance metric that impacts the device's ability to conduct current efficiently. Thus, as detailed in this Petition, a person of ordinary skill in the art ("POSITA") would have been motivated to apply this known design to improve the operation of high-power MOSFETs, where low on-resistance is of critical importance.

In particular, the design would have improved the high-power device of U.S. Patent Pub. No. 2004/0119076 ("Ryu"), which teaches a SiC MOSFET with the same JFET region as the '633 Patent. Ryu was concerned with reducing on-resistance of the device—a design goal that would have been furthered by adopting the source-region layout of Depetro or Choy as discussed in Grounds 1 and 2 of this Petition.

II. MANDATORY NOTICES

A. Real Party-In-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Wolfspeed identifies itself as the real party-in-interest.

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), Purdue asserted the '633 Patent against Wolfspeed in a complaint filed on October 28, 2021. *The Trustees of Purdue Univ. v. Wolfspeed, Inc.*, No. 21-cv-00840 (M.D.N.C.). Ex. 1016. Purdue previously asserted the '633 Patent against STMicroelectronics ("STMicro") in a complaint filed July 14, 2021. *The Trustees of Purdue Univ. v. STMicroelectronics NV et al.*, No. 21-cv-00727 (W.D.T.X.). Ex. 1017. STMicro filed a petition for *inter partes* review of the '633 Patent on December 6, 2021. IPR2022-00252, Paper 1.

C. Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. § 42.8(b)(3) and (4), the designations of counsel and address for service are listed below. Petitioner consents to electronic service at the email addresses below.

LEAD COUNSEL	BACKUP COUNSEL
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51 Madison Avenue, 22nd Floor New York, NY 10010 Tel: (212) 849-7000 Fax: (212) 849-7100	Washington, DC 20005 Tel: (202) 538-8000 Fax: (202) 538-8100 Richard W. Erwine *(pro hac vice application to be filed)* richarderwine@quinnemanuel.com **Postal and Hand Delivery Address:** QUINN EMANUEL URQUHART & SULLIVAN, LLP 51 Madison Avenue, 22nd Floor New York, NY 10010 Tel: (212) 849-7000 Fax: (212) 849-7100

III. STANDING

Wolfspeed certifies that the '633 Patent is available for IPR, and that Wolfspeed is not barred or estopped from requesting review. Purdue filed a complaint alleging infringement of the '633 Patent on October 28, 2021, and service was effectuated no sooner than November 4, 2021. Accordingly, this Petition is timely filed pursuant to 35 U.S.C. § 315(b).

IV. PAYMENT OF FEES

Petitioner authorizes the office to charge Deposit Account No. 505708 for the Petition fee set forth in 37 C.F.R. § 42.15(a), and for any additional fees.

V. IDENTIFICATION OF CHALLENGE AND RELIEF REQUESTED

A. Grounds for *Inter Partes* Review

Wolfspeed requests cancellation of claims 9-11 of the '633 Patent on the following grounds:

Ground 1: U.S. Patent Pub. No. 2004/0119076 ("Ryu") in combination with U.S. Patent No. 6,043,532 ("Depetro") renders obvious claims 9-11.

Ground 2: Ryu in combination with U.S. Patent No. 5,171,705 ("Choy") renders obvious claims 9-11.

B. How the Claims are Unpatentable

An explanation of how the challenged claims of the '633 Patent are unpatentable under the statutory grounds identified above is provided in Section XI.

C. Supporting Evidence

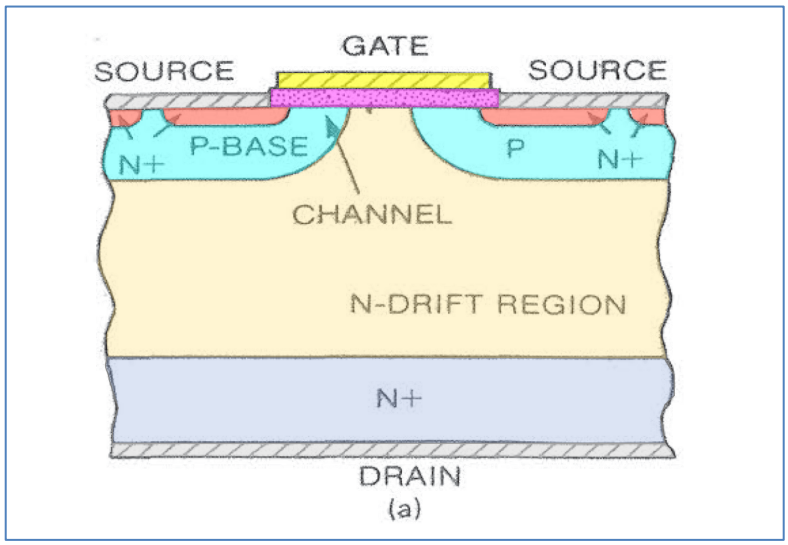
The exhibit numbers of the evidence relied upon and the relevance of the evidence to the challenges raised are provided herein. An exhibit list identifying the exhibits is included *supra*, iv-v. The Petition is accompanied by the declaration of Jack C. Lee, Ph.D., an expert in electrical engineering and semiconductor device physics. Ex. 1010.

VI. TECHNOLOGY BACKGROUND

A. MOSFETs

A MOSFET is a device used for switching and regulating current in electronic circuits. Ex. 1010 ¶ 26. MOSFETs date back to the 1920s, when the concept of establishing a static electric field in a semiconductor material to modulate current flow was first proposed. The conductance of the semiconductor material depends, in part, on the number of free carriers it contains, which can be modified by applying a static electric field in the direction transverse to current flow. The idea of exploiting this so-called "field effect" led to the invention of the JFET in the 1950s and the MOSFET in the 1960s.

Further research in the 1970s led to *power MOSFETs*, which were designed for high-voltage and high-current applications. *Id*. ¶ 27. A conventional vertical power MOSFET is shown below:



Ex. 1008 at 265.

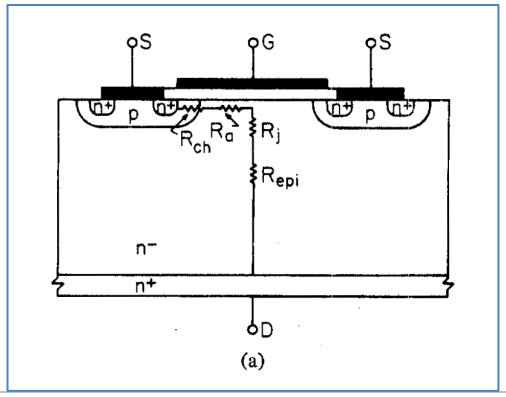
The illustrated device is characterized by vertical current flow from an upper source to a lower drain. Ex. 1010 ¶ 28. The components of the device include a gate electrode (yellow), gate oxide (pink), upper source electrodes (gray), and lower drain electrode (gray). Between the source and drain are a series of semiconductor layers, including an n+ substrate (blue), an n-type epitaxial drift layer (tan), p-type base regions (turquoise), and n+ source regions (red). The letters *n* and *p* refer to the doping of the semiconductor material. In an n-channel MOSFET, current flows from source to drain as electrons, which are more mobile than holes (*i.e.*, the absence of an electron). For this reason, power MOSFETs like the device shown above typically relied on n-type doping for the source, drift region, and substrate.

In conventional power MOSFETs formed of silicon, the p-type wells and n-type source regions were formed using a double-*diffusion* process that involved a first p-type diffusion and a second n-type diffusion. *Id*. ¶ 29. These devices became known as DMOSFETs. In the 1990s, the industry identified SiC as a promising alternative for power MOSFETs. SiC was known to have a lower dopant diffusivity than silicon, and thus required double-*implantation* to form the p-type wells and n-type source regions. The devices thus became known as DIMOSFETs.

During on-state operation of a vertical power MOSFET, the gate terminal is biased, which causes an electric field to form across the oxide layer. *Id*. ¶ 30. The field causes channels to form under the gate, with current flowing first laterally from the source regions and then vertically through the drift layer and into the drain terminal of the device. In the off state, the drift layer blocks any forward voltage applied to the device up to its breakdown voltage.

B. On-Resistance

Vertical power MOSFETs were able to achieve strong performance in terms of switching speed, thermal stability, and input impedance. Ex. 1010 ¶ 31. Ex. 1009 at 1693. A primary design concern, however, was large on-state resistance. *Id*. ("The most important design trade-off for power MOSFETs is that between on-resistance and breakdown voltage"). The on-resistance of a device consists of several components, including: channel resistance (R_{ch}), accumulation resistance (R_a), epi resistance (R_{epi}), and JFET resistance (R_j):



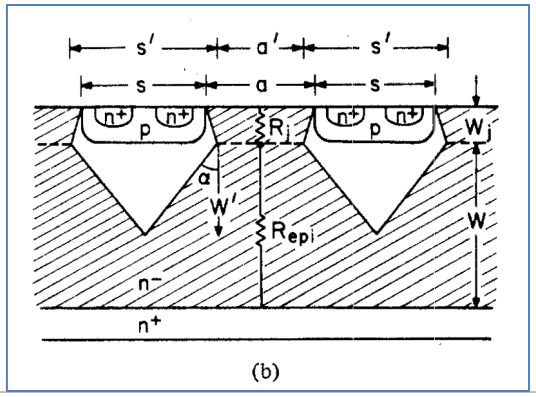
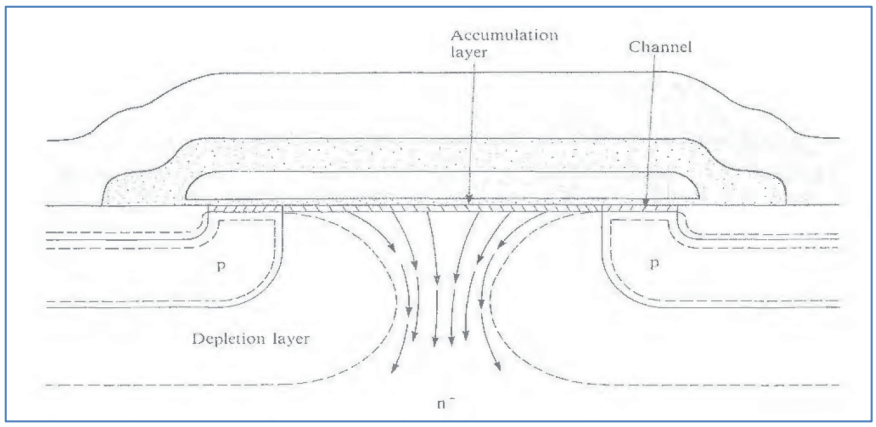


Fig. 1. (a) The four components of on-resistance are shown for a power VDMOS transistor. (b) Definition of R_j and R_{epi}. Current is assumed to flow in the shaded region. The narrowest part is the neck of the JFET.

Id.

The diamond-shaped regions in Figure 1(b) represent depletion regions that form at the interface of the p-well and n- epilayer. Ex. 1010 ¶ 32. A JFET region is formed between the depletion regions that "pinches" current flow from source to drain and thus increases its resistance. Grant illustrates the pinching, or "JFET action" in the image below:

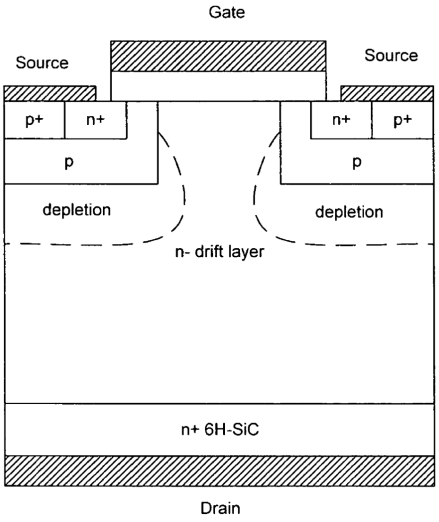


Ex. 1011 at Fig. 3.18.

Grant explains that the "JFET action occurs in the region between the p diffusions" and that the "effect is more severe in high-voltage devices, because the epilayer is more lightly doped and the depletion layers that form at the body-drain junction extend further into the drain." *Id*. at 81. Ryu recognized the same problem in the context of high-power SiC devices:

A further difficulty with DIMOSFETS may be associated with the JFET region of the device. As seen in FIG. 1 depletion region may be formed in the n drift region around the p-well. This depletion region may effectively make the channel length longer than the p-well junction depth as current flow is provided around the depletion region.

Ex. 1003 at [0009], Fig. 1.



Techniques to minimize on-resistance in power MOSFETs were subject to extensive study starting in the 1970s. Ex. 1010 ¶ 34. One technique involved widening the JFET region and thereby reducing the degree of "pinching" from the depletion regions. That approach had drawbacks, however, because it increased the cell size of the device and compromised blocking voltage. *Id.*; Ex. 1003 at [0044]. Grant focused on the drift region of the device and explained that its contribution to on-resistance "should be kept as small as possible." Ex. 1011 at 74. One technique Grant proposed was to increase the donor doping concentration in the drain throats. *Id.* at 83-84.

Ryu proposed another solution: a JFET limiting region that reduced the depletion region under the p-wells and thereby lowered the JFET component of on-resistance. Ex. 1003 at [0039]. The JFET limiting region is shown as element 26a:

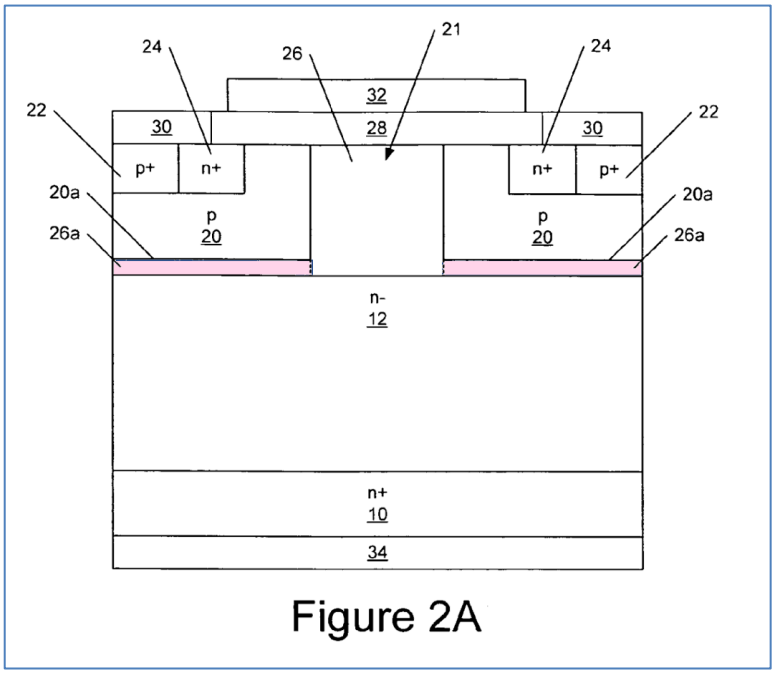


Figure 2A

Id. at Fig. 2A.

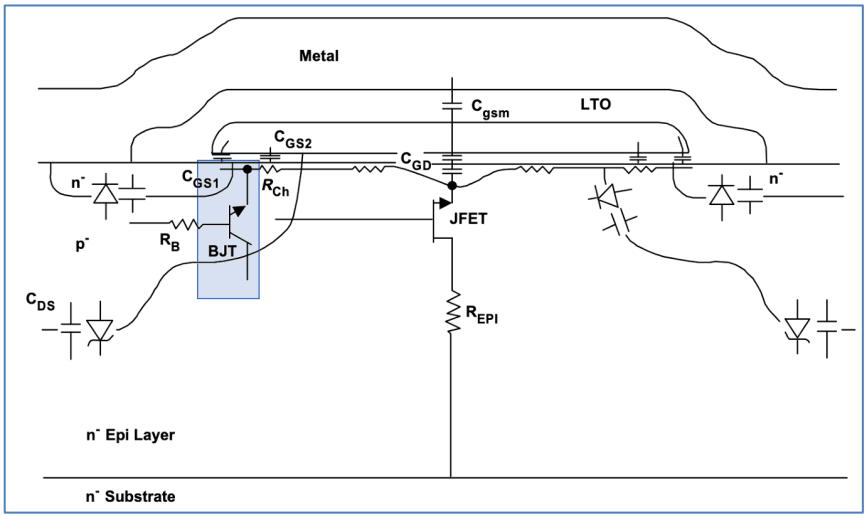
The JFET limiting region reduced the JFET component of on-resistance by relieving the JFET action of the depletion zones. *Id*. at [0044]; Ex. 1010 ¶ 36. This allowed Ryu to reduce the size of the JFET region, which provided a number of benefits. First, it reduced the cell size, and thus increased cell density or number of cells that could be fabricated on a fixed area of the substrate. Second, it shielded the gate oxide from the electric field that forms during the blocking state of the device. This allowed the device to operate at high blocking voltages for long periods of time without the oxide layer degrading. Third, the smaller JFET region reduced the cell pitch, which was known to reduce the channel component of on-resistance. The tradeoff is an increase in the JFET component of on-

resistance that would result from reducing the width of the JFET region. *Id.*; Ex. 1015.

In addition to adjusting the width of the JFET region, it was also known that one could adjust the source-region layout of the device to impact its on-resistance. Ex. 1010 ¶ 37. Hu, for example, explained that "on-resistance can further be minimized … by proper cell layout design." Ex. 1009 at 1693. Williams also recognized the impact of source-region layout on on-resistance and detailed the design tradeoffs associated with various known designs. Ex. 1006 at 16:28-35.

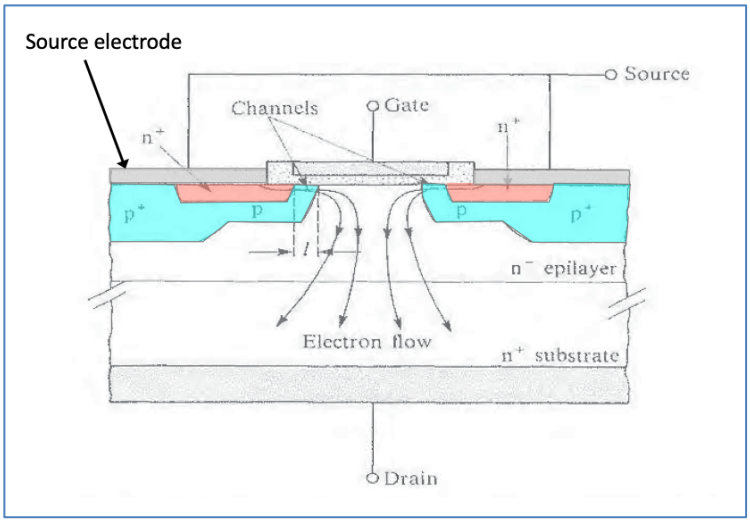
C. Parasitic Bipolar Transistor

The inherent design of a MOSFET includes several parasitic components that can degrade performance. Ex. 1010 ¶ 38. A key parasitic feature of power MOSFETs is a bipolar junction transistor ("BJT") between the source, body, and drain of the device:



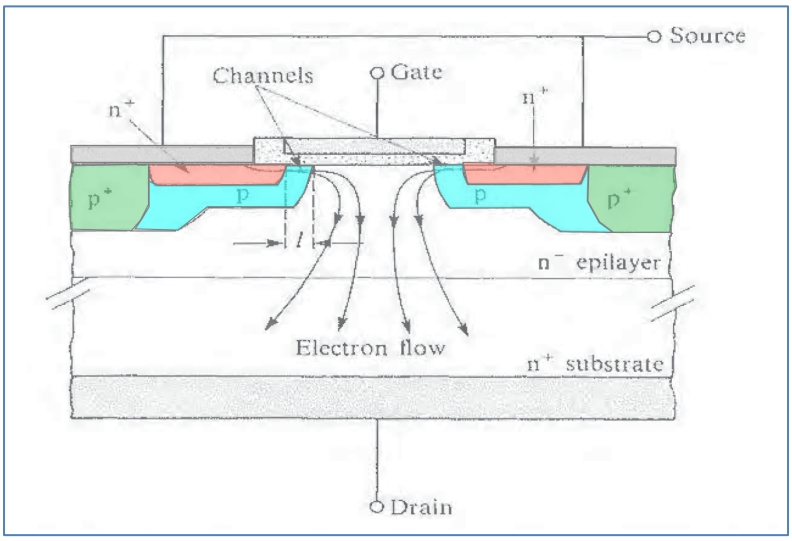
Ex. 1011 at Fig. 3.15; Exs. 1019-1020.

Under certain conditions, the parasitic BJT may be activated, which can lead to unwanted turn-on of the device and premature breakdown. *Id*. at 81; Ex. 1010 ¶ 39. Thus, a known design consideration for power MOSFETs was to prevent the parasitic transistor from turning on. One known technique to accomplish this was to short the n-type source region to the p-type base region using source metallization, which was commonly referred to as a source contact, source electrode, or ohmic contact. Ex. 1008 at 266 ("This parasitic bipolar transistor must be kept inactive during all modes of operation of the power MOSFET. To accomplish this, the *P*-base region is short-circuited to the *N*+ emitter region by the source metallization"); Ex. 1006 at 6:5-14 ("The source-to-body short prevents conduction and snapback break-down of the parasitic NPN bipolar transistor"). Figure 1.11 of Grant shows an example source electrode overlying—and therefore shorting—the n+ source region and p-well body region:



Ex. 1011 at Fig. 1.11.

Grant further teaches that current at the base of the parasitic transistor is subject to a resistance R_{bb}. *Id*. at 89. The resistance causes a voltage drop which, if it exceeds a threshold, activates the transistor. To reduce the resistance and prevent turn-on of the transistor, Grant explains that a p+ diffusion is used "to connect the body region back to the source contact." *Id*. Figure 1.11 of Grant is annotated below to show the p+ diffusion in green:



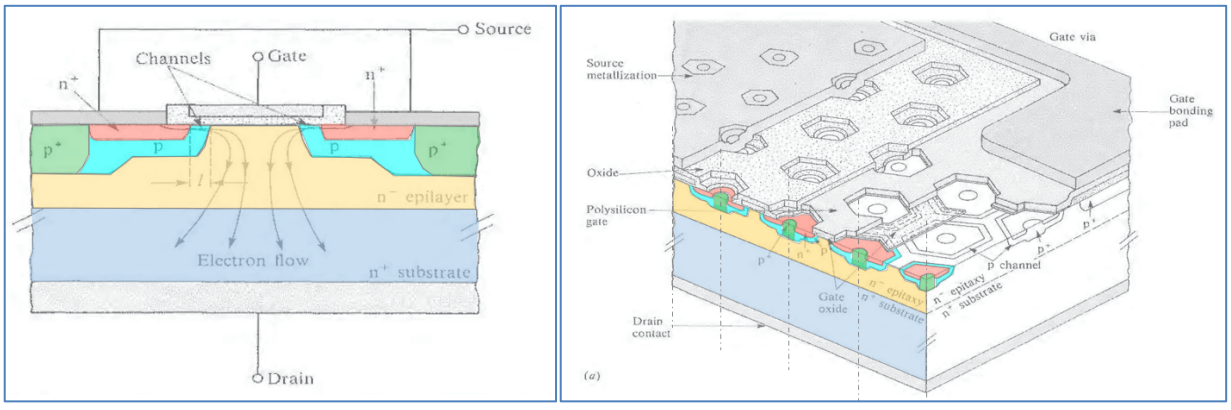
Id. at Fig. 1.11.

Grant teaches the p+ body contact is "an important part of VDMOS FET design." *Id*. at 90. Indeed, it was well known in the art that the design and doping concentration of the p+ region impacted ruggedness of the device and its ability to withstand turn-on of the parasitic bipolar transistor. Ex. 1010 ¶ 41; Ex. 1006 at 16:28-35. Numerous references recognized the importance of p+ body contacts in terms of preventing turn-on, including Depetro, which teaches spaced-apart

strongly doped p-type body contacts in the source region, along with a strongly doped p-type section formed at the edge of the body to draw current away from the parasitic BJT and thus prevent it from turning on. *Id*. at 2:14-26, 3:45-54.

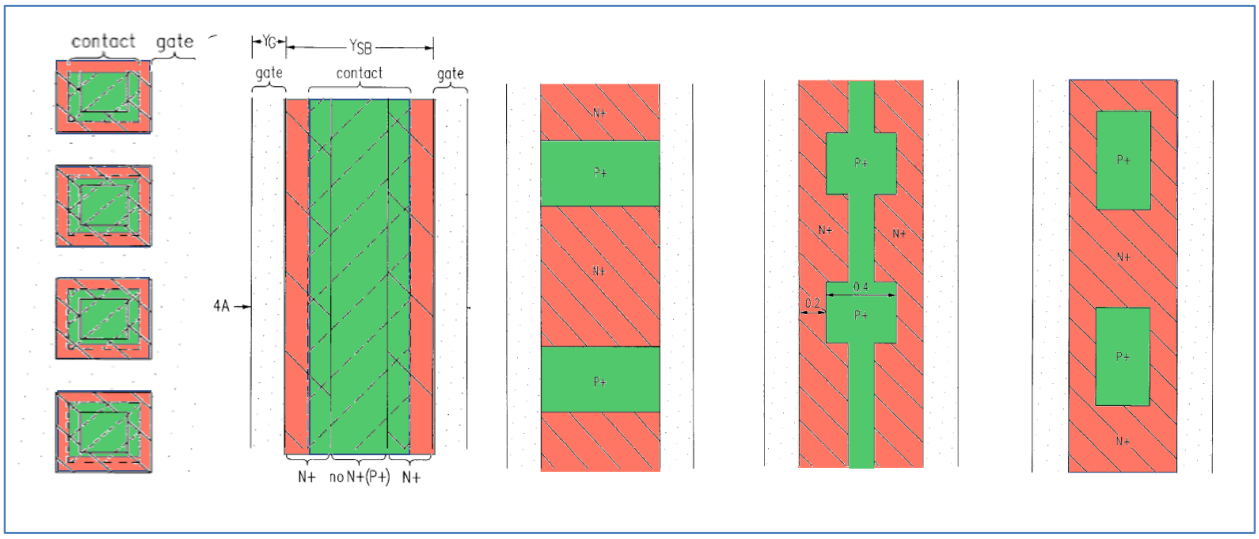
D. Unit Cells and Source Region Layouts

The prior art frequently illustrates MOSFETs using cross-sectional diagrams that show the layers of the device from bottom to top. Ex. 1010 ¶ 42. The depiction of a single MOSFET is referred to as a "unit cell." A POSITA would have understood, however, that an individual unit cell represents multiple parallel cells fabricated to form a single MOSFET. This is illustrated in the images below. The first image shows a unit cell, annotated to show its n+ substrate (blue), n- drift layer (tan), p-wells (turquoise), n+ source regions (red), and p+ base contacts (green). The second image shows the unit cell repeated multiple times to form a MOSFET:



Ex. 1011 at Figs. 1.11, 1.13(a).

In the right-hand image above, the MOSFET device is formed as a series of hexagonal cells. Ex. 1010 ¶ 43. Additional patterns for forming the n+ source regions and p+ base contacts were well known in the art, including square cells, stripes, alternating strips, and islands that are either connected or spaced-apart. *Id*. These designs are illustrated in Williams:



Ex. 1006 at Figs. 4, 19; Ex. 1014 at Figs. 1-3.[2]

A POSITA would have understood that each layout would have a similar cross-section, with the p+ body contacts formed within the n+ source region. Ex. 1010 ¶ 44. Thus, the layout for one MOSFET would have been applicable to other MOSFETs having similar cross-sections. A POSITA also would have understood that a layout could be chosen to balance the design considerations detailed above,

[2] As discussed in Section VII.B, the '633 Patent states that the alleged invention can be implemented with various known layouts, including hexagonal cells, strips, and spaced apart islands. Ex. 1001 at 5:37-41, 8:7-11.

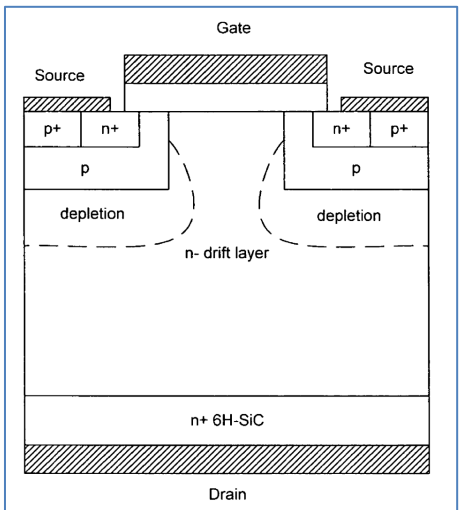
including low on-resistance and preventing turn-on of the parasitic BJT to avoid premature breakdown. Williams explains this point as follows: "The design can be selected to maximize the N+ source perimeter (to achieve the lowest possible resistance) or to maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device), or to compromise between the two." Ex. 1006 at 16:28-35.

E. SiC MOSFETs

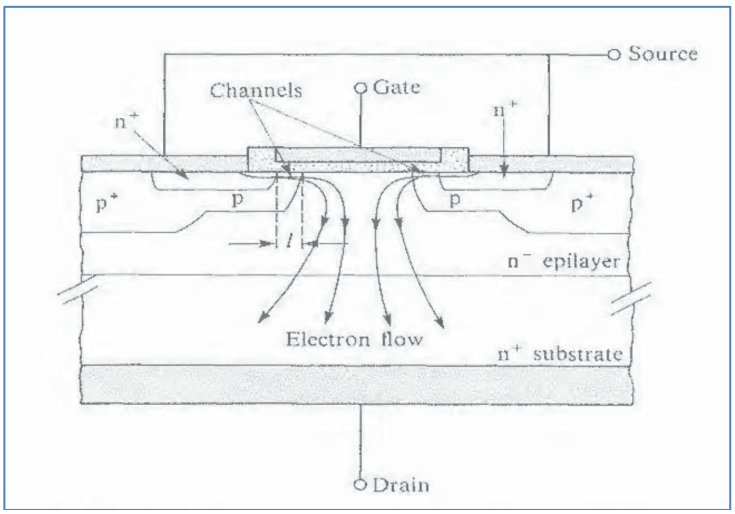
As noted above, early power MOSFETs were designed in silicon, which was widely available in the 1970s and 1980s. Ex. 1010 ¶ 45. In the 1990s, researchers and industry participants began to develop power MOSFETs in SiC. *Id*. The SiC devices were seen as a promising alternative because they could withstand high power and temperatures, which made them well-suited for power applications. *Id*.; Ex. 1013 at 4:22-43; Exs. 1021-1023. As SiC technology developed, it became apparent that many of the design techniques and structures known for silicon devices were also applicable to SiC. The prior art teaches fabrication methods for translating silicon designs into SiC, including epitaxial growth, patterning, and ion implantation. *Id*.; Ex. 1012 at 1:56-63.

Using these techniques, those in the field adapted known silicon designs to SiC. Ex. 1010 ¶¶ 46-47. Ryu, for example, discloses a prior-art SiC device that was a variation of silicon designs. Ex. 1003 at [0006] ("[T]he vertical DIMOSFET

structure, illustrated in FIG. 1, is a variation of the diffused (DMOSFET) structure employed in silicon technology."). As shown below, the SiC device in Figure 1 of Ryu includes the same basic structure as the silicon device in Grant:

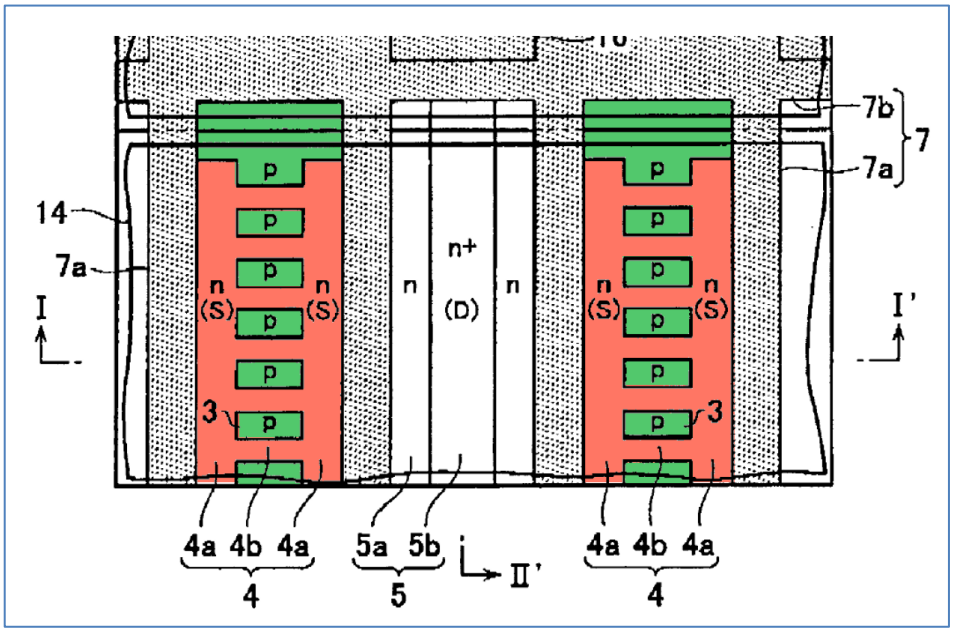


Ex. 1003 at Fig. 1



Ex. 1013 at Fig. 1.11

The devices also suffered from the same JFET action and its impact on on-resistance, which Ryu addressed with the JFET limiting region formed under the p-wells as discussed above. Ex. 1003 at [0039]. In addition to the vertical structure, it was also recognized that design principles for the source-region layout of a silicon device were applicable to SiC. Ex. 1010 ¶ 48. Nakayama, for example, teaches the known island layout with spaced-apart p-type base contacts in an n-type source region, and further explains that the layout can be implemented in silicon or SiC, with the known benefit of reducing on-resistance:



Ex. 1007 at Fig. 11; [0045], [0057].

As detailed in the Grounds of this Petition, a POSITA would have been motivated to apply these known source-region layouts to the SiC MOSFET of Ryu to reduce its on-resistance and improve its operation.

VII. THE '633 PATENT

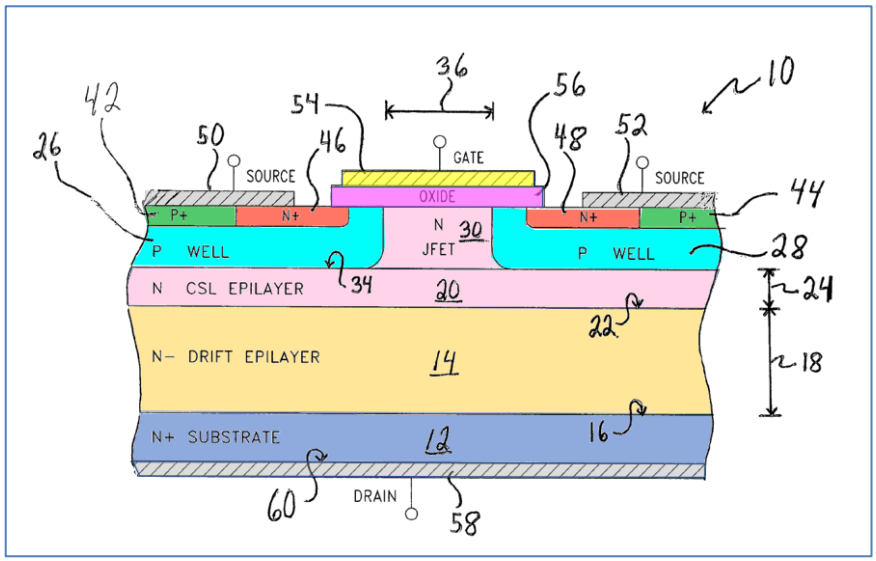
A. Overview

The '633 Patent is titled *High-Voltage Power Semiconductor Device*. Ex. 1001. The patent was filed on January 23, 2006 and issued on March 3, 2009. *Id.* The patent was originally assigned to Purdue Research Foundation, and names James A. Cooper and Asmita Saha as inventors. *Id.*

B. Specification

The '633 Patent is directed to MOSFETs for high-power applications. *Id.* at 1:18-36. According to the patent, the devices are capable of providing high-

blocking voltages and decreased specific on-resistance to improve efficiency. *Id*. Figure 1 illustrates a cross-section of the device:



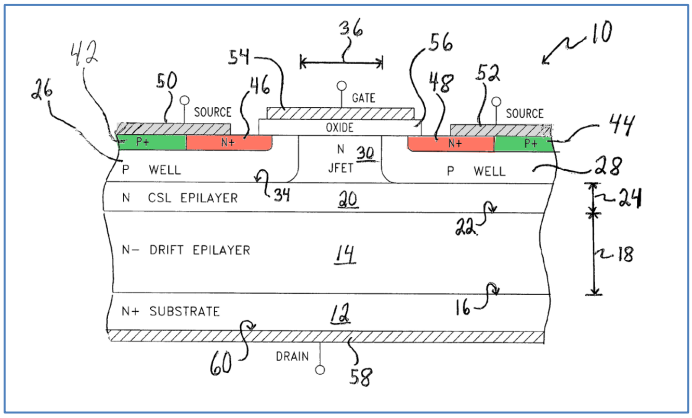
Id. at Fig. 1.

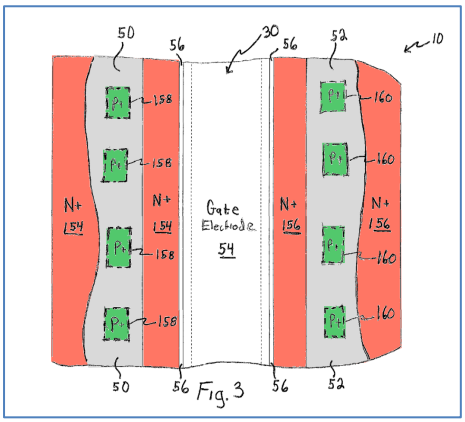
The device 10 includes a substrate 12 with successive semiconductor layers formed on it. *Id*. at 4:4-6. The substrate may be formed of SiC. *Id*. at 1:44-45. On the frontside 16 of the substrate 12 is a drift layer 14. *Id*. at 4:21-22. In the embodiment of Figure 1, the drift layer 14 is doped with N-type impurities to an N- concentration. *Id*. at 4:39-31. On the front side 22 of drift layer 14 is a current spreading layer 20 ("CSL"). *Id*. at 5:1-3.[3] The CSL is doped to an N-type concentration greater than that of the drift layer 14. *Id*. at 5:12-14.

[3] The CSL is not an element of the challenged claims; however, Wolfspeed has provided a description of it for completeness.

On the front side 34 of the CSL are two doped semiconductor wells or base regions 26 and 28, with a JFET region 30 formed between them. *Id*. at 5:23-26. In the embodiment of Figure 1, the wells are doped to a P concentration, whereas the JFET region 30 is doped with N-type impurities to an N concentration. *Id*. at 5:42-45. In some embodiments, the JFET region 30 may have a width of less than about three microns. *Id*. at 1:65-67.

Formed on each P-well are source regions 46, 48 and base-contact regions 42, 44. *Id*. at 6:63-66. In the Figure 1 embodiment, the source regions 46, 48 are doped to an N+ concentration, whereas the base contact regions 42, 44 are doped to a P+ concentration. *Id*. In the embodiment of Figure 3, the P+ base contacts 158 are formed as spaced apart islands surrounded by the N+ source regions 154, with a source electrode 50, 52 over the source region. *Id*. at Fig. 3. Viewing the cross-section above with the overhead view of Figure 3, one can visualize the layout of the n+ source region, p+ base contacts, and source electrodes:





Id. at Figs. 1, 3.

In addition to the island embodiment, the '633 Patent states that the alleged invention can be implemented in other known source-region layouts, including hexagonal cells or alternating strips. *Id*. at 5:37-41, 8:7-11. In the illustrated embodiments, the device is a vertical MOSFET with source electrodes on the upper surface and a drain electrode on the lower surface. *Id*. at Fig. 1. The patent explains, however, that the alleged invention is not limited to vertical devices. *Id*. at 2:26-28.

C. Prosecution History

The '633 Patent was filed as Application No. 11/338,007 on January 23, 2006. Ex. 1002. Application claim 12, which issued as challenged claim 9, is reproduced below:

> 12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
>
> a semiconductor substrate;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
>
> a first source region;
>
> a second source region; and
>
> a JFET region defined between the first source region and the second source region , the JFET region having a width less than about three micrometers.

Id. at 207.

On April 4, 2007, the Examiner issued a Non-Final Rejection finding claim 12 anticipated by U.S. Patent Publication No. 2003/0227052 A1 ("Ono"). *Id*. at 131-34. The Examiner relied on Ono's disclosure of a DMOSFET with the same layer and region structure as claimed. *Id*.

On August 6, 2007, the Applicant submitted amendments that modified claim 12 to require the substrate was formed of "silicone-carbide" *[sic]*. *Id*. at 112. The claim was also amended to require "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other" and "a plurality of second base contact regions" with similar requirements. *Id*. In accompanying remarks, the Applicant argued that Ono did not anticipate claim 12 as amended, and that it would not have been obvious to incorporate Ono's JFET region in a SiC substrate because doing so would allegedly "reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose (*i.e.*, high power applications)." *Id*. at 117-19. Notably, the Applicant did *not* argue that the first and second plurality of spaced-apart base contact regions distinguished the claim from the prior art. *Id*.

On October 12, 2007, the Examiner issued a Final Rejection finding claim 12 obvious based on Ono, U.S. Patent No. 6,573,534 ("Kumar"), and U.S. Patent No. 6,137,139 ("Zeng"). *Id*. at 84-86. The Examiner rejected the Applicant's arguments about implementing Ono's DMOSFET in SiC, finding that the

combination would "improve breakdown voltage and reduce ON resistance as is known in the art." *Id*. at 95-96. Given these "known advantages" of silicon carbide, the Examiner found that a POSITA would have found it obvious to use. *Id*.

The Applicant submitted further amendments on March 12, 2008. *Id*. at 71. The Applicant amended claim 12 to require a "first source electrode" and "second source electrode," each formed over the respective first and second source regions. *Id*. The amendments also required the first and second base contact regions to be spaced apart "in a direction "parallel to the longitudinal axis defined by" the first and second source electrodes. *Id*. In accompanying remarks, the Applicant repeated its prior arguments about implementing the device of Ono in SiC. *Id*. at 74-78. In particular, the Applicant argued that forming the JFET region of Ono on a SiC substrate would render the device unsatisfactory or inoperable for its intended purpose. *Id*. And again, the Applicant did not place any particular emphasis on the limitations directed to spaced apart base contact regions or their relationship with the source electrode. *Id*.

In response to the Applicant's amendments, the Examiner found claim 12 allowable in a Non-Final Rejection submitted June 25, 2008. *Id*. at 39. Despite the fact that the Applicant did not rely on the claimed arrangement of spaced-apart base-contact regions, the Examiner found the limitation missing in the prior art of

record. *Id*. at 48-49. After the Applicant amended the other claims, the Examiner issued a further Notice of Allowance on December 17, 2008. *Id*. at 8.

D. Claims

Wolfspeed challenges claims 9-11, reproduced below:

Claim 9	
9[a]	A double-implanted metal-oxide semiconductor field-effect transistor comprising:
9[b]	a silicon-carbide substrate;
9[c]	a drift semiconductor layer formed on a front side of the semiconductor substrate;
9[d]	a first source region;
9[e]	a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
9[f]	a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
9[g]	a second source region;
9[h]	a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
9[i]	a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
9[j]	a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.
Claim 10	

10	The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer.
Claim 11	
11	The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

E. Priority Date

The '633 Patent is related to Provisional Application No. 60/646,152, filed January 21, 2005. *Id*. The '152 Application does not provide priority support for challenged claims 9-11 of the '633 Patent. Independent claim 9 requires a first and second plurality of base contact regions spaced apart from each other in a direction parallel to the longitudinal axis defined by a first and second source electrode. Ex. 1001 at claim 9. It also requires a "JFET region having a width less than about three micrometers." Claims 10 and 11 include the same requirements through dependency. *Id*. at claims 10-11.

The spaced-apart configuration of base-contact regions corresponds to Figure 3 of the '633 Patent. *Id*. at 7:52-59. That embodiment—along with any other description of spaced-apart base-contact regions—is not described in the '152 Application. Ex. 1018 at 7-8. The '152 Application also fails to disclose a JFET region width that is less than about three micrometers. *Id*.

Accordingly, the priority date of challenged claims 9-11 is the patent application filing date, January 23, 2006.[4]

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA as of January 23, 2006 would have had an undergraduate degree in electrical engineering and 2-3 years of experience in MOSFET design, with knowledge of different semiconductor materials, including SiC. Less work experience may be compensated by a higher level of education. Ex. 1010 ¶¶ 65-72. The same level of skill would apply for an earlier priority date of April 26, 2004 or January 21, 2005. *Id*.

IX. CLAIM CONSTRUCTION

The claim terms in this proceeding are interpreted under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Wolfspeed contends that the challenged claims should receive their ordinary and customary meaning as understood by a POSITA in the context of the patent and prosecution history. Wolfspeed reserves the right to pursue alternative constructions in the related district court proceeding, including that the challenged claims are indefinite

[4] Even if the claims were entitled to the filing date of the provisional application, the references relied upon in this Petition would still qualify as prior art. The same is true if Purdue is entitled to the April 2004 conception date identified in the provisional. Ex. 1018 at 3.

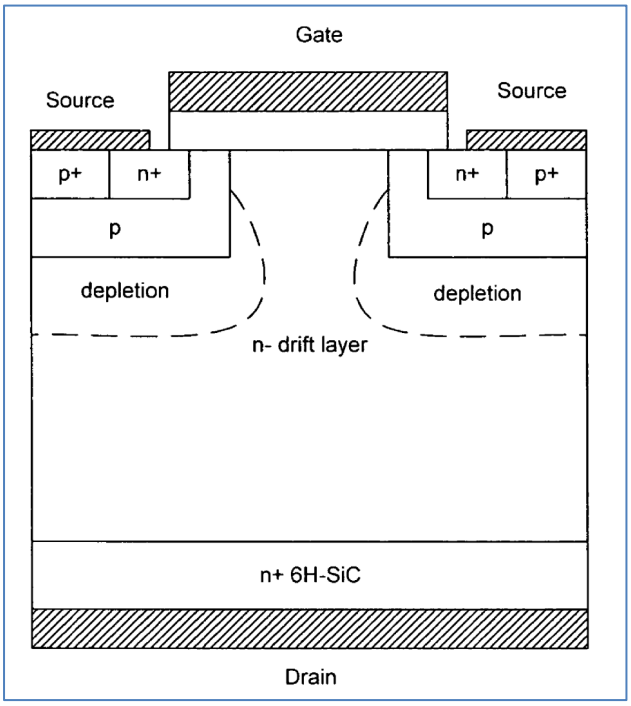
under 35 U.S.C. § 112. Wolfspeed reserves the right to address any construction raised by Purdue in this or another proceeding.

X. OVERVIEW OF THE PRIOR ART

A. U.S. Patent Pub. No. 2004/0119076 ("Ryu")

Ryu is a patent application publication assigned to Wolfspeed and titled, *Vertical JFET Limited Silicon Carbide Power Metal Oxide Semiconductor Field Effect Transistors*. Ex. 1003. Ryu was filed on October 30, 2003 and published on June 24, 2004. *Id*. It therefore qualifies as prior art under 35 U.S.C. §§ 102(b) and (e).

Ryu is directed to structures and fabrication techniques for high-power SiC MOSFETs, with a particular focus on vertical double-implanted devices. *Id*. at [0003]-[0004]. Ryu explains that a difficulty in these devices "may be associated with the JFET region." *Id*. at [0009]. Ryu illustrates the problem in the prior-art embodiment of Figure 1, which shows a "depletion region may be formed in the n drift region around the p-well":



Id. at Fig. 1.

Ryu explains that the "depletion region may effectively make the channel length longer than the p-well junction depth as current flow is provided around the depletion region." *Id*. at [0009]. The longer channel length results in a higher on-resistance for the device, thus degrading its performance. *Id*. Thus, Ryu proposes a SiC device and fabrication technique to reduce on-resistance. *Id*. at [0039]. The device is designed to reduce the depletion region that forms around the p-wells. *Id*. Reducing the depletion region shortens the effective channel length and thereby reduces on-resistance. *Id*. It also allows the width of the JFET gap to be reduced, which leads to increased cell density, increased shielding of the oxide layer in the

blocking state, and reduced cell pitch. *Id*. at [0044]. Figure 2A illustrates a cross-section of Ryu's device:

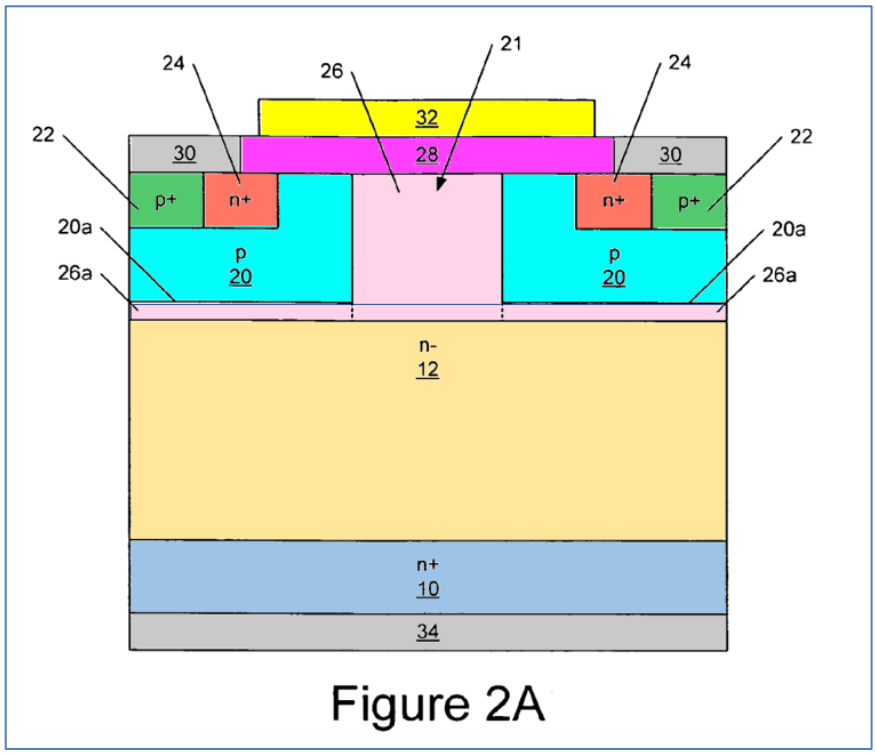


Figure 2A

Ex. 1003 at Fig. 2A.

The device includes an n+ base layer 10, which Ryu teaches may comprise a SiC substrate. *Id*. at [0040]. Formed on the substrate 10 is a drift layer 12 with a relatively lower n- concentration. *Id*. On the front side of the drift layer is a region 26 doped with n-type impurities having a higher concentration than the drift layer. *Id*. at [0041]. The lower end of region 26 extends laterally to form a "JFET limiting region" 26a, which serves to reduce the depletion region in the JFET. *Id*. P-wells 20 are implanted into the epitaxial drift layer on either side of region 26. *Id*. The upper portion of region 26 extends between the p-wells 20 and defines a

gap 21 that Ryu defines as the "JFET region." *Id*. at [0044]. Ryu teaches that the JFET region 21 may have a width between about 1 and 10 micrometers, owing to the reduction in the depletion region around the p-wells. *Id*.

Implanted into p-wells 20 are n+ regions 24 and p+ base contacts 22. *Id*. at [0045]. The n+ source regions 24 and p+ base contacts 22 are shorted by a source contact 30, which is formed of nickel, platinum, aluminum, or another suitable material to "provide an ohmic contact to both the p+ regions 22 and the n+ regions 24." *Id*. at [0047]. A drain contact 34 is formed on the lower portion of the device. *Id*. Ryu's device, therefore, includes the same cross-section features as the device of the '633 Patent:

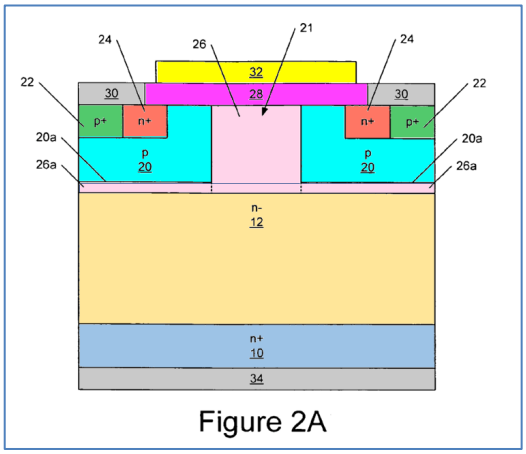
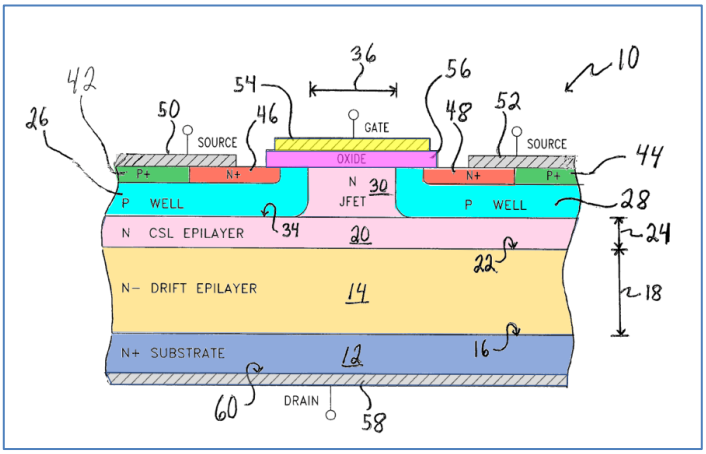


Figure 2A

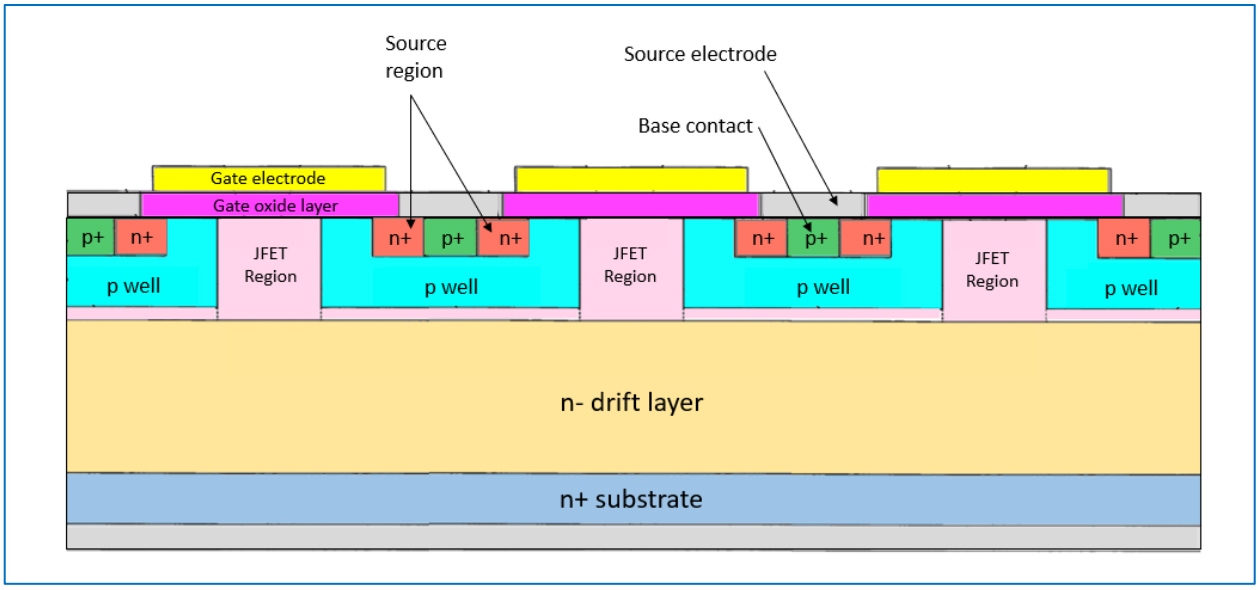
Ex. 1003, Ryu at Fig. 2A



Ex. 1001, '633 Patent at Fig. 1

Figure 2A of Ryu illustrates the device as a unit cell, which is common in the art. *Id*. at [0051]. Ryu teaches, however, that the unit cell represents multiple devices having the same structure and formed on a common substrate. *Id*. ("While

FIGS. 2A, 2B and 3 illustrate embodiments of the present invention as discrete devices, as will be appreciated by those of skill in the art, FIGS. 2A, 2B and 3 may be considered unit cells of devices having multiple cells."). The demonstrative below illustrates how a series of multiple unit cells would appear:



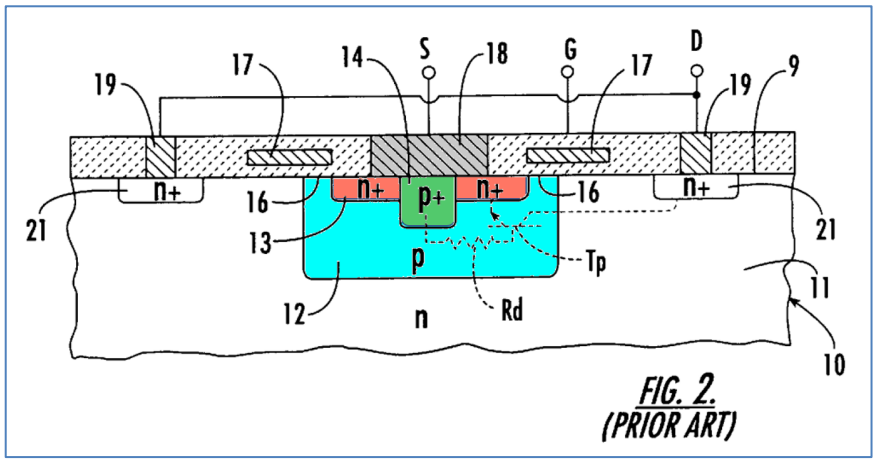
Ex. 1010 ¶ 78.

B. U.S. Patent No. 6,043,532 ("Depetro")

Depetro is titled, *DMOS Transistor Protected Against Snap-Back*. Ex. 1004. Depetro issued on March 28, 2000, and therefore qualifies as prior art under 35 U.S.C. § 102(b).

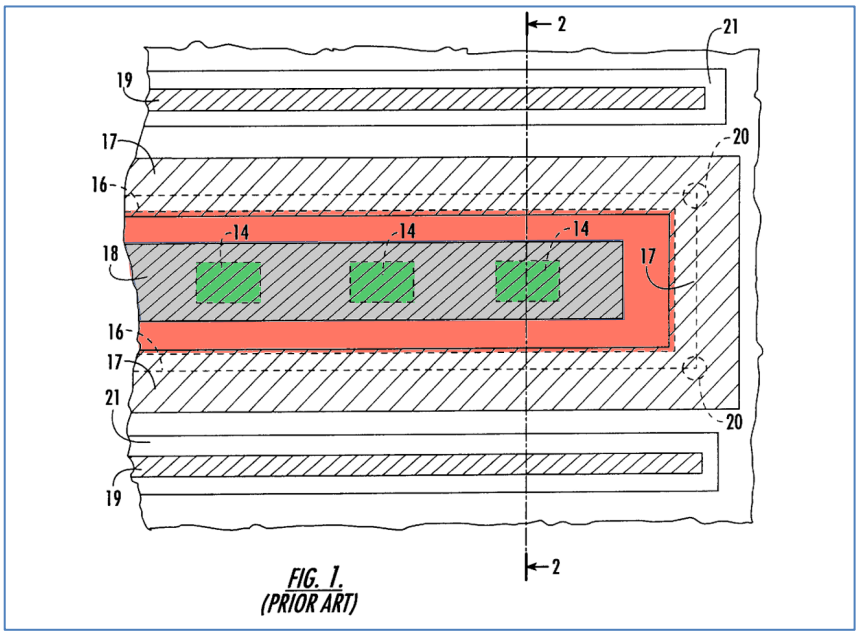
Depetro teaches double-diffused MOSFETs for high-power applications, with designs that are applicable to both lateral and vertical devices. *Id*. at 1:10-12, 4:44-50. Figure 2 of Depetro illustrates a prior-art device that includes a p-type

body region 12, n+ source region 13, p+ body contact 14, and source electrode 18 that shorts the n+ source region and p+ body contacts:



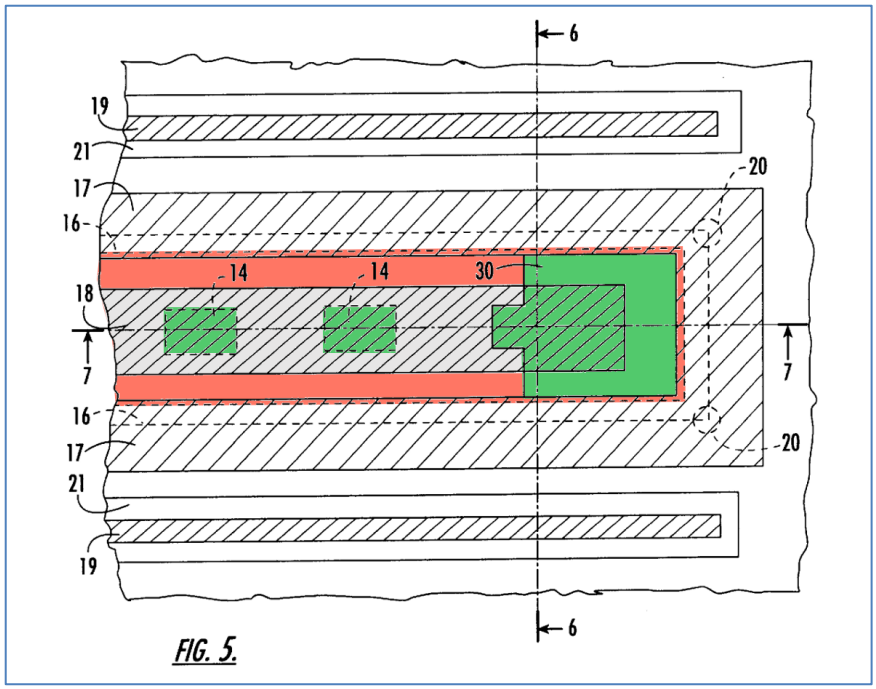
Id. at Fig. 2.

Figure 1 of Depetro illustrates the layout for the n+ source region 13 and p+ base contacts 14, which are spaced apart along a longitudinal axis defined by the source electrode 18:



Id. at Fig. 1.

Notably, Depetro recognizes that the device shown in Figures 1-2 was part of the prior art. *Id*. Depetro seeks to improve the device by introducing a strongly doped p+ region at the corner of the body to draw current and prevent turn on of the parasitic BJT shown in Figure 2. *Id*. at 2:4-26; 3:45-66. Figure 5 illustrates how the region 30 is integrated into the prior-art device of Figure 2, which retains the same arrangement of spaced-apart p+ base contacts:



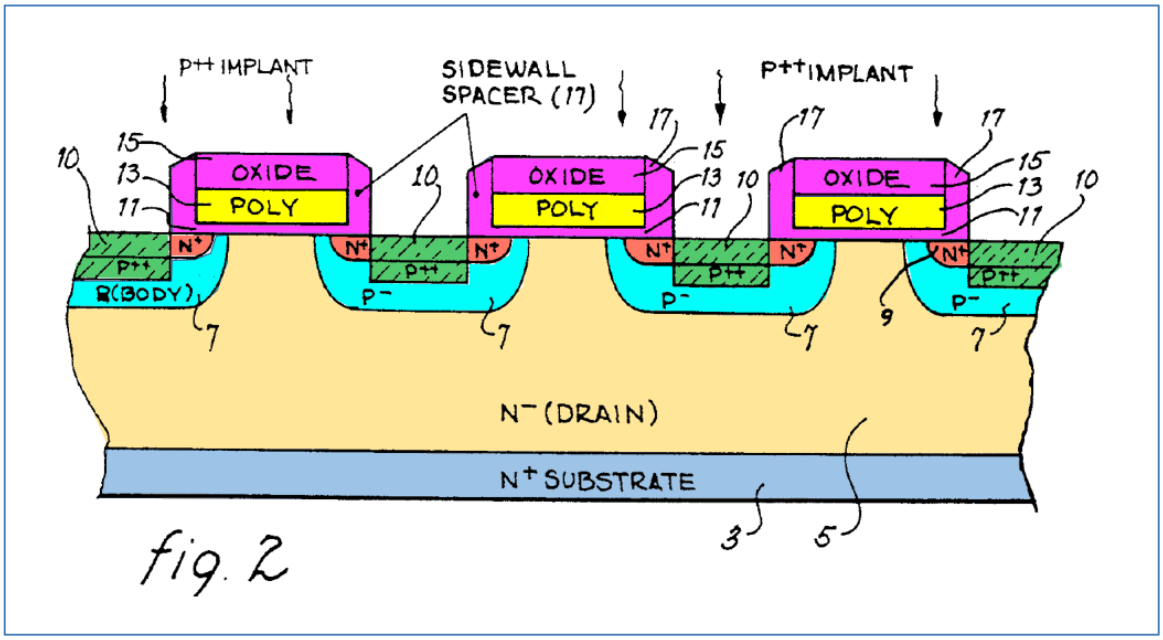
Id. at Fig. 5.

Finally, as noted above, Depetro teaches that the disclosed design principles are applicable to both lateral and vertical MOSFETs. *Id*. at 4:44-50 ("Moreover, the invention applies not only to LDMOS transistors, but also to VDMOS transistors, that is, those with vertical current flow, and can be implemented with the same advantages...").

C. U.S. Patent No. 5,171,705 ("Choy")

Choy is titled, *Self-Aligned Structure and Process for DMOS Transistor*. Ex. 1005. Choy issued on December 15, 1992, and therefore qualifies as prior art under 35 U.S.C. § 102(b).

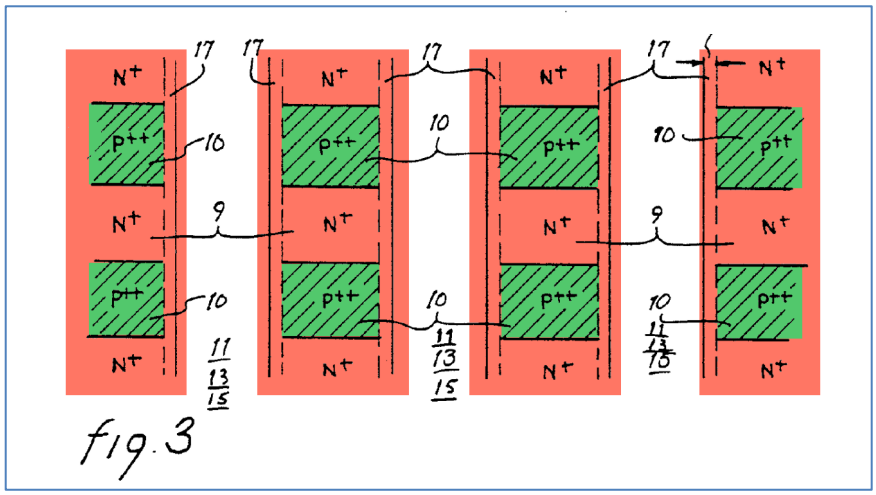
Choy teaches a double-implanted vertical MOSFET with improved body contact to reduce turn-on of a parasitic bipolar transistor. *Id*. at 1:20-34, 2:64-3:40. The MOSFET includes an n+ substrate 3, an n- drift region 5, implanted p-body wells 7, implanted n+ source regions 9, and p++ body contacts 10:



Id. at Fig. 2.

Choy explains that the p-type body contacts are important for preventing turn-on of the parasitic bipolar transistor formed between source, body, and drain.

Id. at 1:22-34. In one embodiment, Choy forms the p-type body contacts 10 as a series of spaced-apart islands in the source region 9:



Id. at Fig. 3.

Finally, Choy teaches that the p++ body contacts and n+ source regions are shorted within each stripe. *Id*. at 3:32-40 ("The (P++) body contact regions 10 are partly blocked by an additional mask which leaves alternating (N+) source regions 9 and (P++) body contact regions 10 along the peripheries of the overlapping gate structures 11, 13 and 15. Following conventional metal deposition and definition, these regions will be electrically shorted to each other in each stripe.").

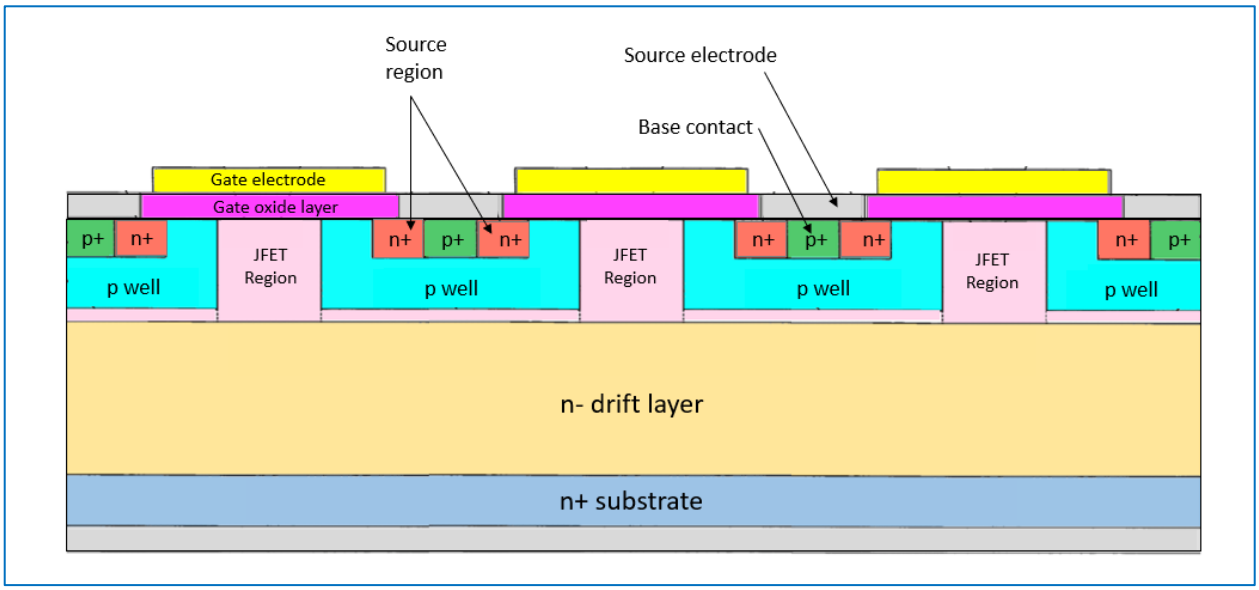
XI. DETAILED EXPLANATION OF GROUNDS FOR INVALIDITY

Pursuant to 35 U.S.C. § 314(a), the following grounds establish a reasonable likelihood that Petitioner will prevail with respect to the challenged claims.

A. Ground 1: Ryu and Depetro Render Obvious Claims 9-11

1. Overview

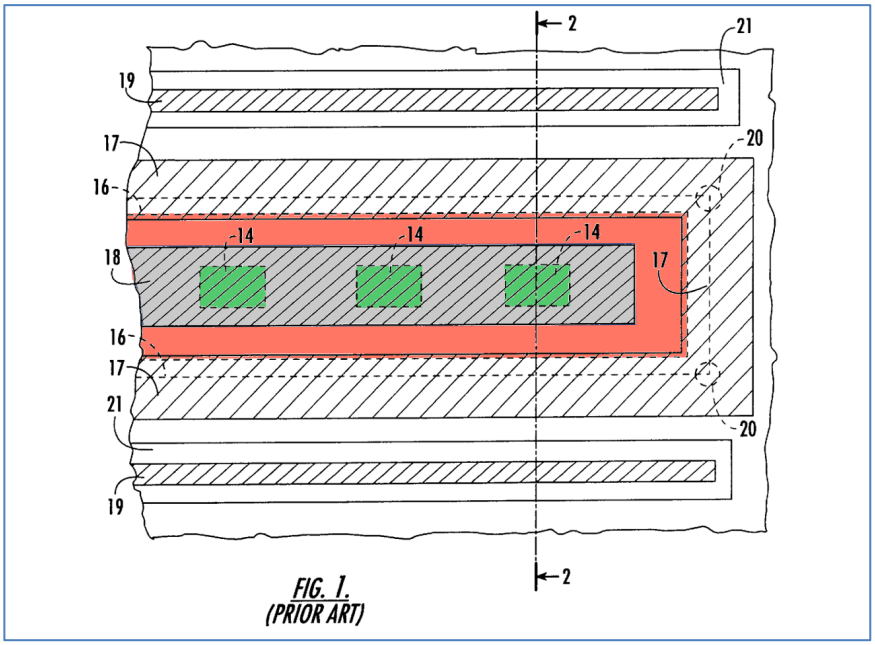
The combined teachings of Ryu and Depetro render obvious claims 9-11 of the '633 Patent. Ex. 1010 ¶ 89. Ryu discloses a SiC vertical DIMOSFET with a cross-sectional structure that includes a substrate, drift layer, first and second n+ source regions, first and second p+ base contact regions defined in the source regions, first and second electrodes formed over the source regions and base contact regions, and a JFET region with a width of less than three microns. *Id.* Ryu illustrates these elements in the unit cell of Figure 2A, which Ryu explains may represent multiple cells in a single device as shown below:



Id.; Ex. 1003 at Fig. 2A, [0051].

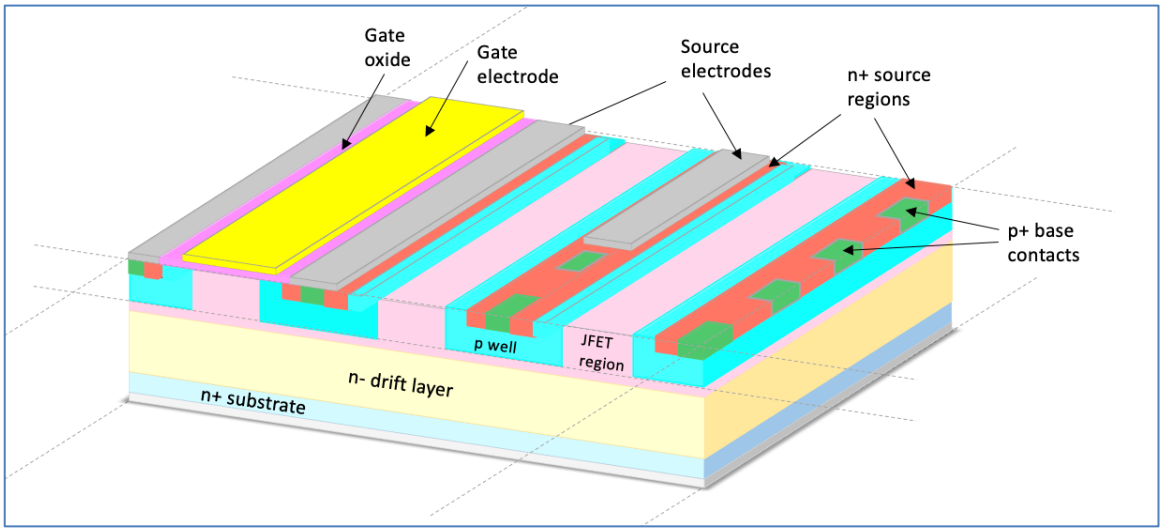
Ryu does not detail the topside layout of its n+ source regions and p+ base contact regions, leaving it to a POSITA to choose an appropriate design. Ex. 1010

¶ 90. Depetro teaches a layout that includes an n+ source region with a plurality of p+ base contact regions spaced apart from each other along a longitudinal axis defined by a source electrode:



Ex. 1004 at Fig. 1.

When the source-region layout of Depetro is applied to the DIMOSFET of Ryu, the resulting structure includes each limitation of challenged claims 9-11. In particular, the p+ base contacts of Ryu would be formed in the n+ source region as a plurality of spaced-apart islands defined along the longitudinal axis of the source electrode, as shown in the demonstrative image below:



Ex. 1010 ¶ 91.[5]

Further, a POSITA would have been motivated to combine the teachings of Ryu and Depetro because it would have reduced the on-resistance of the resulting device, while preventing turn-on of the parasitic bipolar transistor and maintaining a high blocking voltage. Ex. 1010 ¶ 92. The combination of Ryu and Depetro is detailed in the following sections. The teachings of the references are addressed in Sections XI.A.2-4. Motivation to combine and reasonable expectation of success are addressed in Sections XI.A.5-6.

[5] The demonstrative includes certain elements cut away to show the underlying layers. Ex. 1010 ¶ 91, n. 4. In an assembled device, the source electrodes, gate oxide layers, and gate electrodes would extend across the top surface of the device as shown in the left-most side of the image. *Id*.

2. Claim 9

a) Limitation 9(a): "A double-implanted metal-oxide semiconductor field-effect transistor"

Ryu discloses limitation 9(a). Ex. 1010 ¶ 93. Ryu is directed to structures and fabrication methods for SiC MOSFETs. Ex. 1003 at Abstract. Ryu teaches that the disclosed SiC MOSFETs are formed using masks to successively implant the P-wells and N+ source regions. *Id*. at [0053], [0054]. First, "a mask 100 is formed and patterned on the n-type epitaxial layer 26 and impurities are implanted into the n-type epitaxial layer 26 to provide the p-wells 20." *Id*. Then "the mask 100 is removed and a mask 104 is formed and patterned and n-type impurities are implanted utilizing the mask 104 to provide the n+ regions 24." *Id*. A POSITA would have understood that the successive implantation steps result in a double-implanted MOSFET as claimed. Ex. 1010 ¶ 93. This is confirmed by Ryu's discussion of vertical doubly implanted MOSFETs that are formed using the same successive implantation technique. *Id*.; Ex. 1003 at [0006]; Fig. 1.

b) Limitation 9(b): "a silicon-carbide substrate"

Ryu discloses limitation 9(b). Ex. 1010 ¶ 94. Ryu teaches an embodiment of the disclosed MOSFET in Figure 2A that includes "an optional n+ layer 10 of silicon carbide." Ex. 1003 at [0040]. Ryu explains that layer 10 may be "an implanted layer or region, an epitaxial layer or a substrate." *Id*. at [0040], [0053]. The silicon-carbide substrate is annotated in blue in the image below:

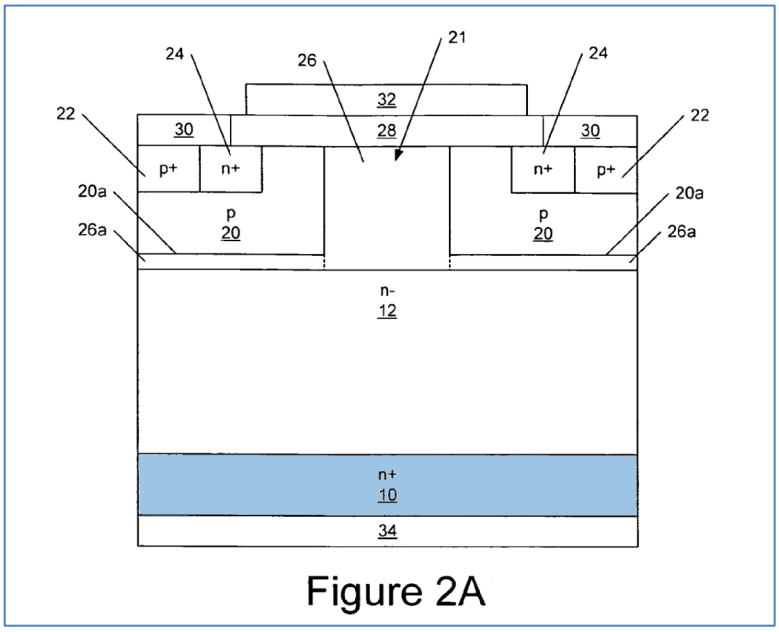


Figure 2A

Id. at Fig. 2A.

c) Limitation 9(c): "a drift semiconductor layer formed on a front side of the semiconductor substrate"

Ryu discloses limitation 9(c). Ex. 1010 ¶ 95. Ryu teaches that "a lightly doped n- drift layer 12 of silicon carbide" is formed on the silicon-carbide substrate 10. Ex. 1003 at [0040]. In some embodiments, the drift layer has a carrier concentration of about 10^{14} to about 5×10^{16} cm^{-3} and a thickness of about 5 to 150 microns. *Id*. The drift layer 12 is annotated in tan in the image below:

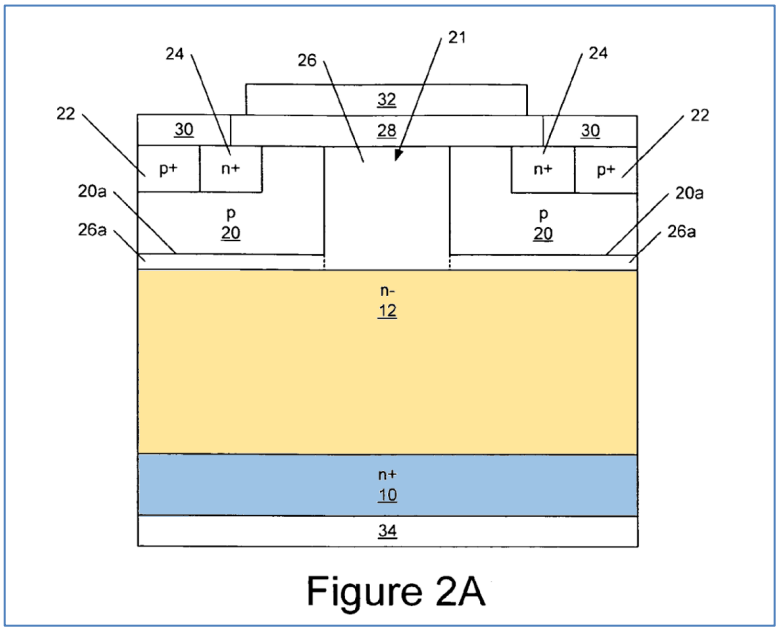


Figure 2A

Id. at Fig. 2A.

d) Limitation 9(d): "a first source region"

Ryu discloses limitation 9(d). Ex. 1010 ¶ 96. Ryu teaches that "Regions of n+ silicon carbide 24 … are disposed within the p-wells 20." Ex. 1003 at [0045]. A POSITA would have understood that the n+ region 24 is a "source region" as claimed because it interfaces with source contact 30 and is formed in the p-wells 20. *Id*. at [0047]. The first source region 24 is annotated in red in the image below, along with the p-well 20 annotated in turquoise:

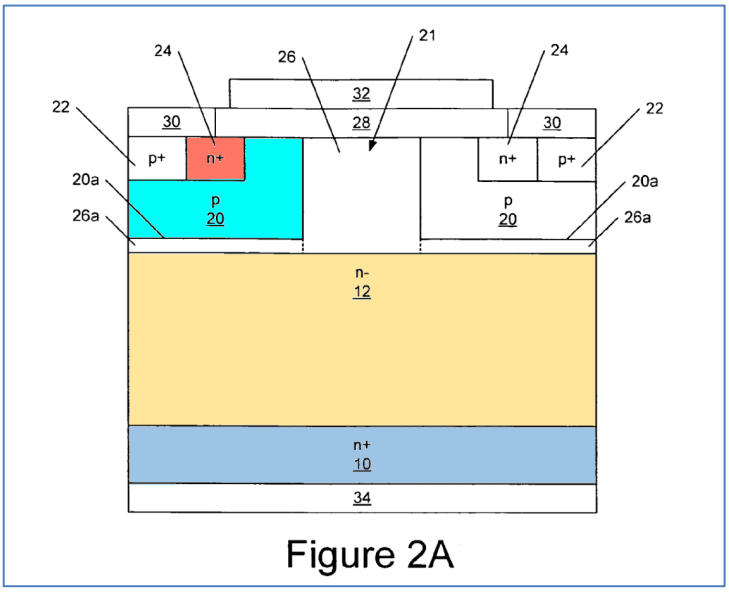
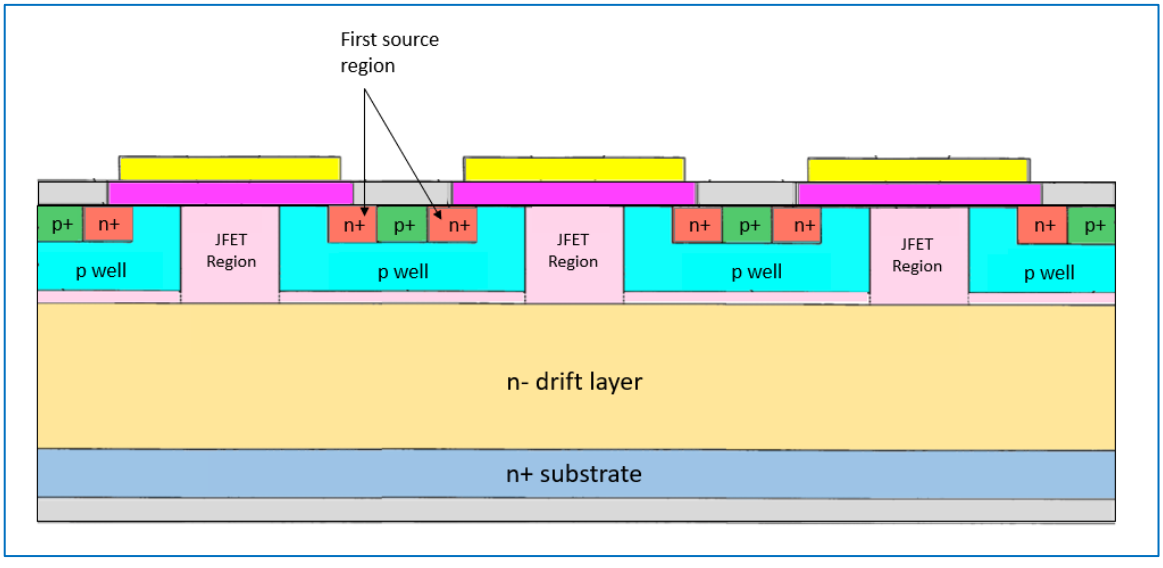


Figure 2A

Id. at Fig. 2A.

As detailed above, Ryu teaches that the unit cell of Figure 2A represents multiple cells having the same structure and formed on a common substrate. *Id*. at [0051]. In the multiple-cell device, each n+ source region would have the structure shown in the demonstrative below:



Ex. 1010 ¶ 97.

e) Limitation 9(e): "a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis"

Ryu in combination with Depetro discloses limitation 9(e). Ex. 1010 ¶ 98. Ryu teaches that the source contact 30 is formed over the n+ source region 24 and p+ base contact 22. Ex. 1003 at [0047]. The source contact 30 is made of nickel, titanium, platinum, aluminum, or another suitable material "to provide an ohmic contact to both the p+ regions 22 and the n+ regions 24." *Id.* A POSITA would have understood that the ohmic contact is an electrode that provides an electrical interface to the source region of Ryu's MOSFET. Ex. 1010 ¶ 98. The first source electrode is shown in gray in the unit cell of Figure 2A and the multiple-cell demonstrative image below:

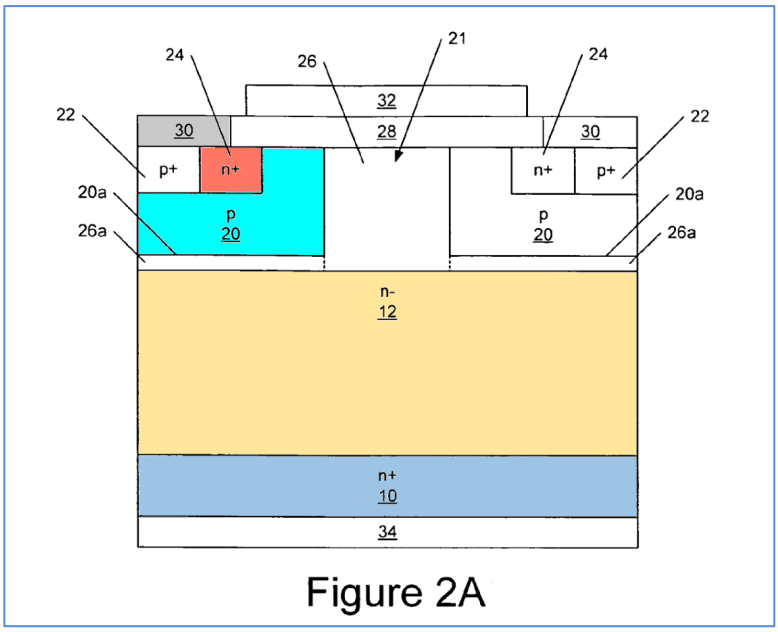
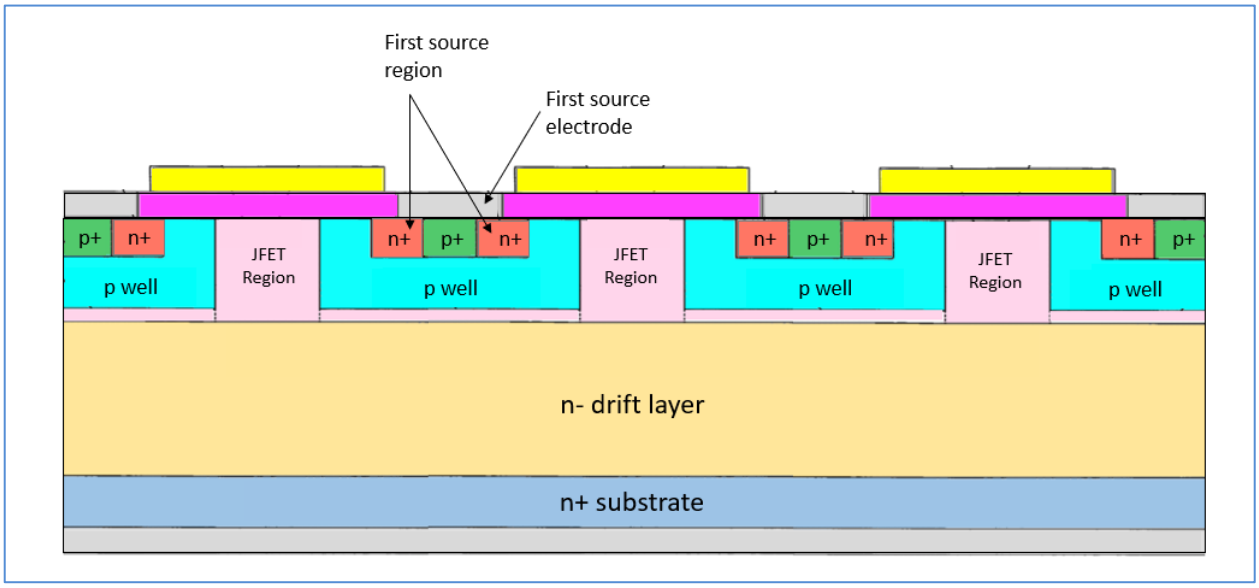


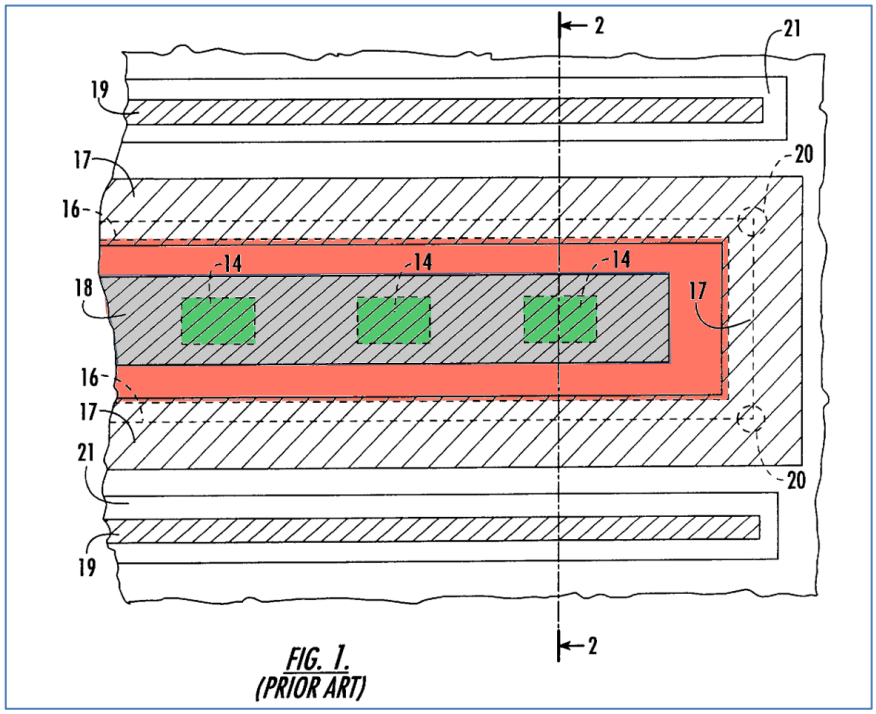
Figure 2A

Ex. 1003 at Fig. 2A.



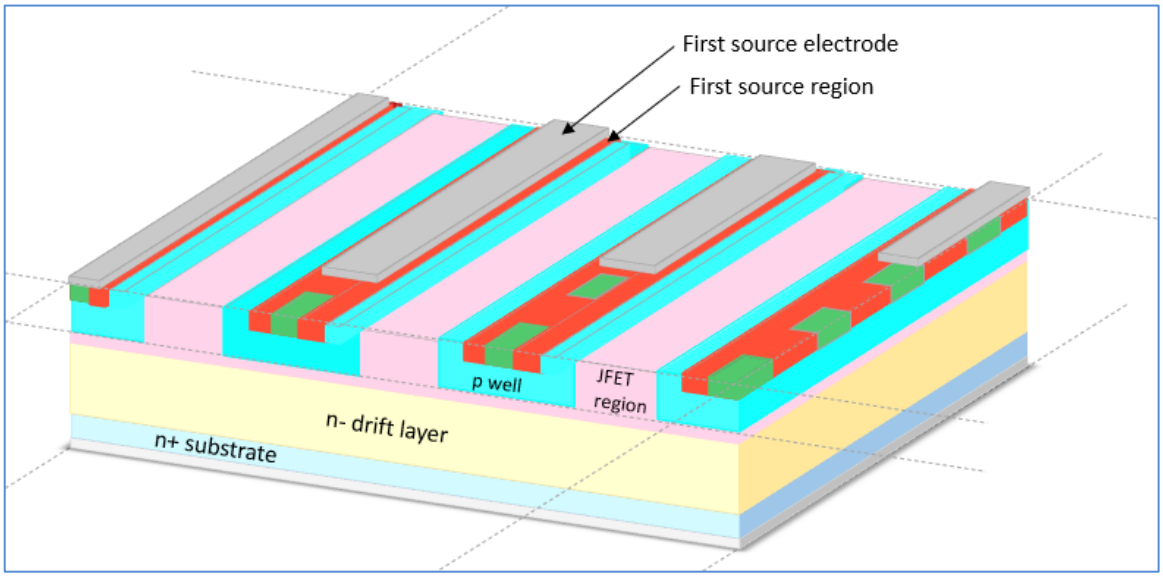
Ex. 1010 ¶ 89.

A POSITA would have understood that the source electrode in Ryu extends into the page with respect to the cross-section images above. *Id.* ¶ 99. He also would have understood that, when the source-region layout of Depetro is applied to the device of Ryu, the source electrode would define a longitudinal axis into the page. *Id.* The source-region layout of Depetro is illustrated in the image below. It includes an n+ source region with p+ base contacts spaced apart along a longitudinal axis defined by source electrode 18:



Id. at Fig. 1.

When the source-region layout of Depetro is applied to Ryu, the source contact 30 of Ryu would extend along the topside of the device and thereby define a longitudinal axis as shown for the source electrode 18 of Depetro. Ex. 1010 ¶ 100. Thus, the resulting device would meet the requirements of limitation 9(e) as shown in the demonstrative below:



Id.[6]

f) Limitation 9(f): "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode"

Ryu in combination with Depetro discloses limitation 9(f). Ex. 1010 ¶ 101. Ryu teaches a first p+ region 22 implanted into the p-well 20 and positioned in the n+ source region 24. Ex. 1003 at [0045]. A POSITA would have understood that the p+ region 22 is a base contact region as claimed because it extends into the p-well 20 and is contacted by the source electrode 30. Ex. 1010 ¶ 101. The first base contact region 22 is annotated in green in the image below:

[6] Three of the source electrodes are cut away to show the underlying structure.

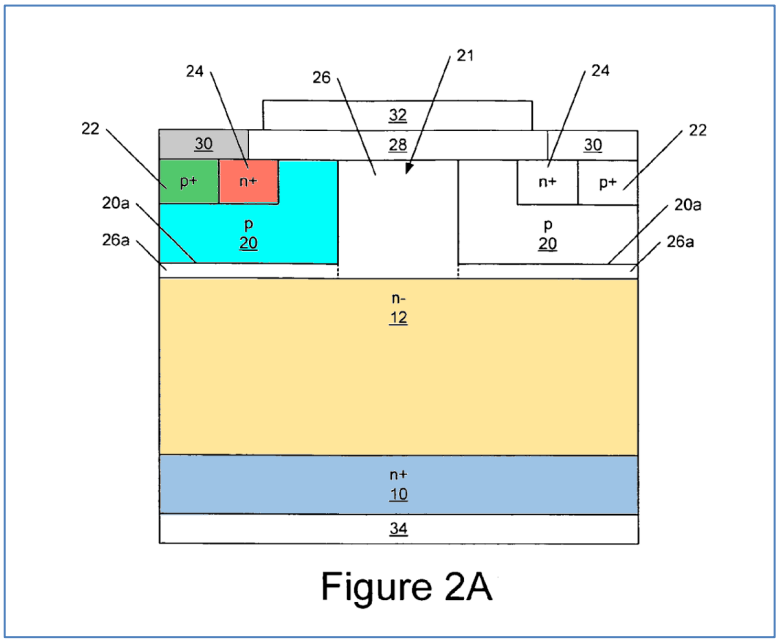
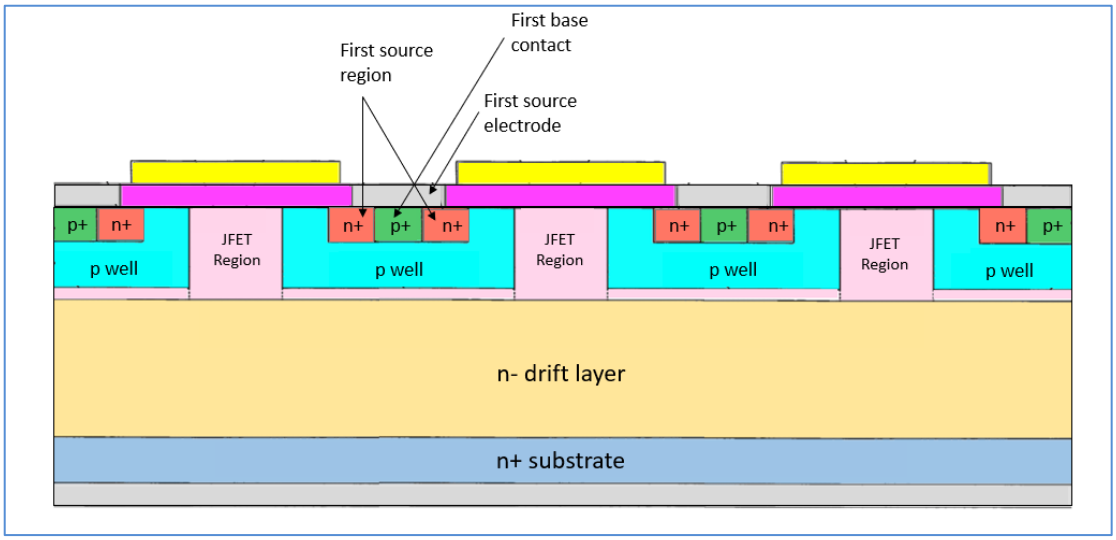


Figure 2A

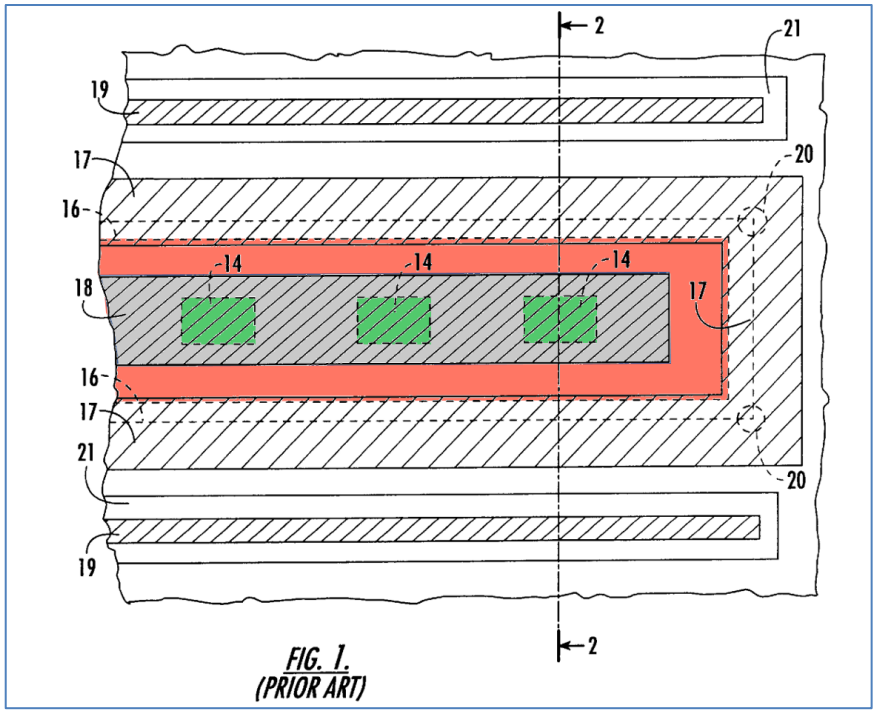
Ex. 1003 at Fig. 2A.

As detailed above, Ryu explains Figure 2A is a unit cell that represents a multiple-cell device, in which the p+ base contacts are surrounded by the n+ source region. *Id*. at [0051]. This is shown in the demonstrative below:



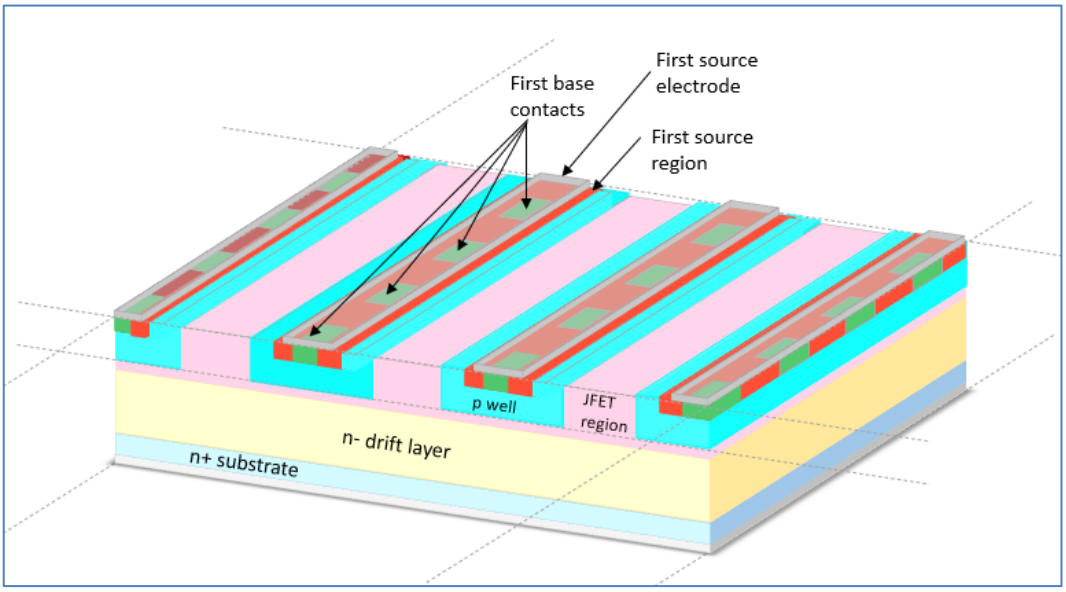
Ex. 1010 ¶ 102.

Although Ryu does not disclose the topside geometry of the device, Depetro teaches a layout in which a plurality of p+ base contacts 14 are spaced apart within the n+ source region 13 in a direction parallel to the longitudinal axis defined by the source electrode 18:



Id. at Fig. 1.

When modified based on the teachings of Depetro, Ryu's p+ base contact regions would be formed as a plurality of regions that are defined in the source region and spaced apart from each other in a direction parallel to the longitudinal axis defined by the source electrode. Ex. 1010 ¶ 104. The resulting device would meet the requirements of limitation 9(e) as shown in the demonstrative below:



Id.[7]

g) Limitation 9(g): "a second source region"

Ryu discloses limitation 9(g). Ex. 1010 ¶ 105. As detailed above, Ryu explains that "Regions of n+ silicon carbide 24 … are disposed within the p-wells 20," and a POSITA would have understood that the n+ regions 24 are "source regions" as claimed. *Id.*; Ex. 1003 at [0045], [0047], [0006]. The second source region is shown in red in both the unit cell of Figure 2A and the multiple-cell demonstrative image below:

[7] The source electrodes are lightened to show the underlying base contacts. *Id.*

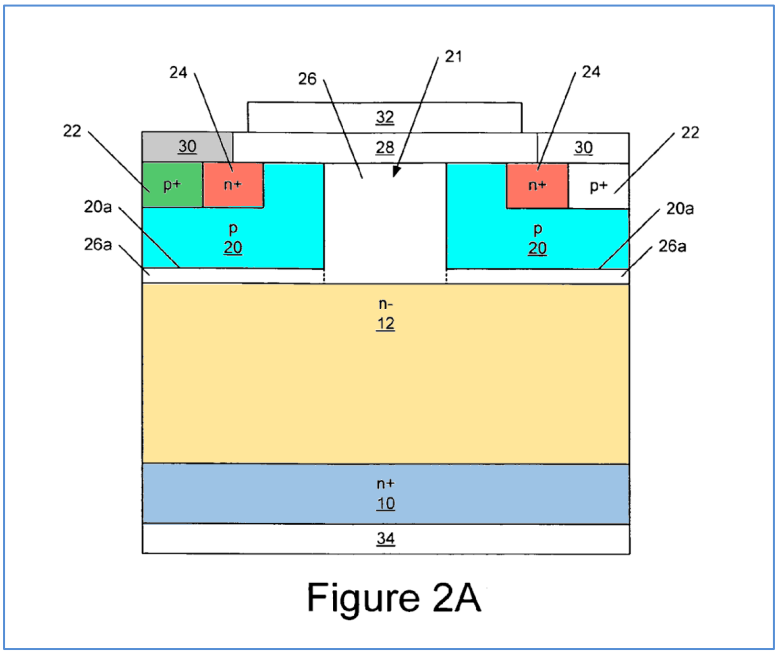
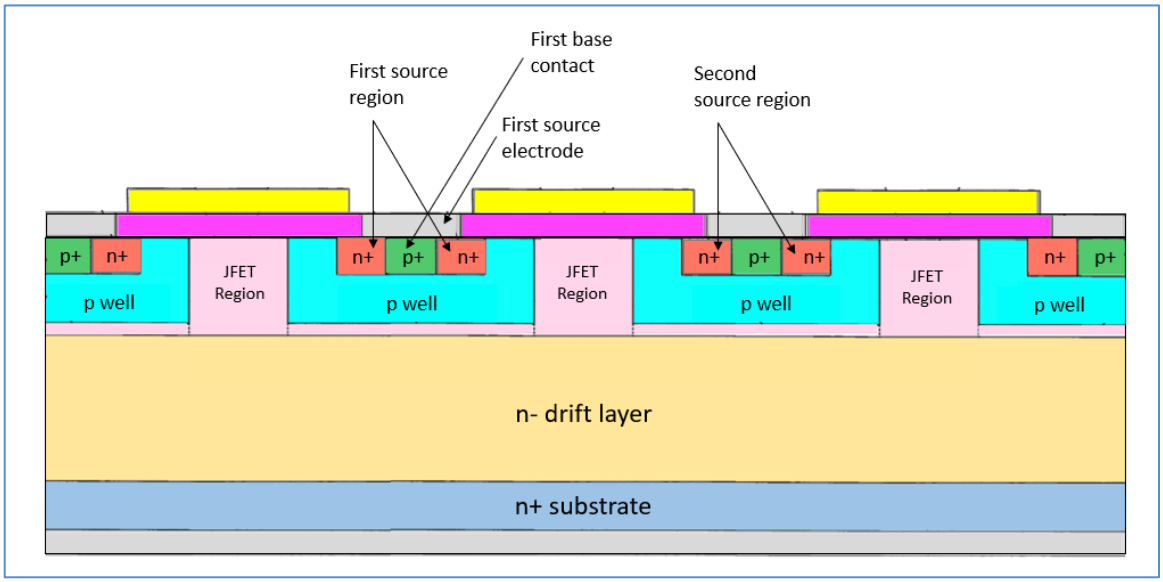


Figure 2A

Id. at Fig. 2A.



Ex. 1010 ¶ 105.

h) Limitation 9(h): "a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis"

Ryu in combination with Depetro discloses limitation 9(h). Ex. 1010 ¶ 106. Ryu explains that a source contact 30 is formed over the second n+ source region 24 to form an ohmic contact with the source region. Ex. 1003 at [0047]. The second source electrode 30 is annotated in gray the unit cell of Figure 2A and the multiple-cell demonstrative image below:

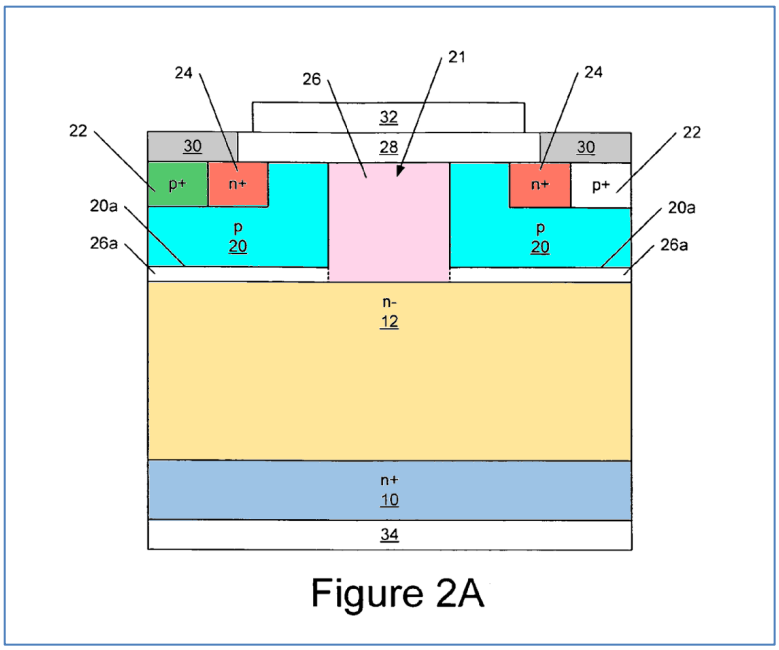
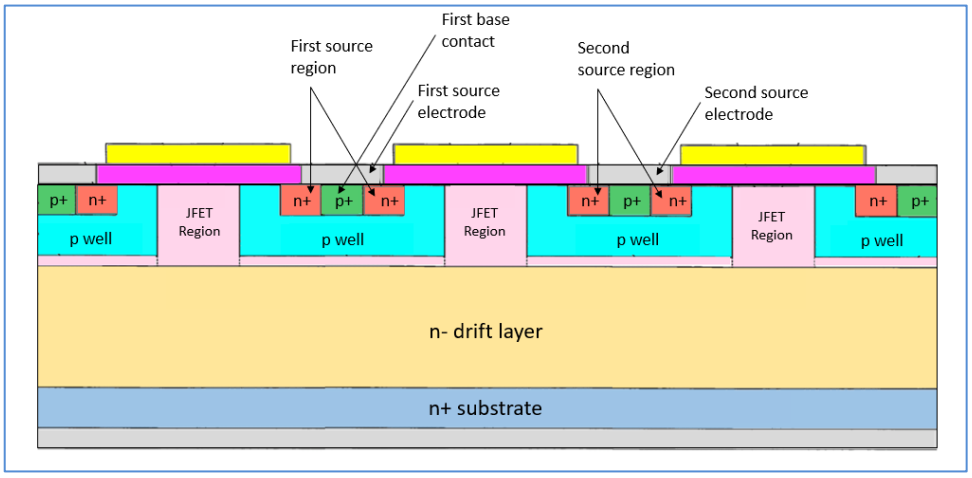


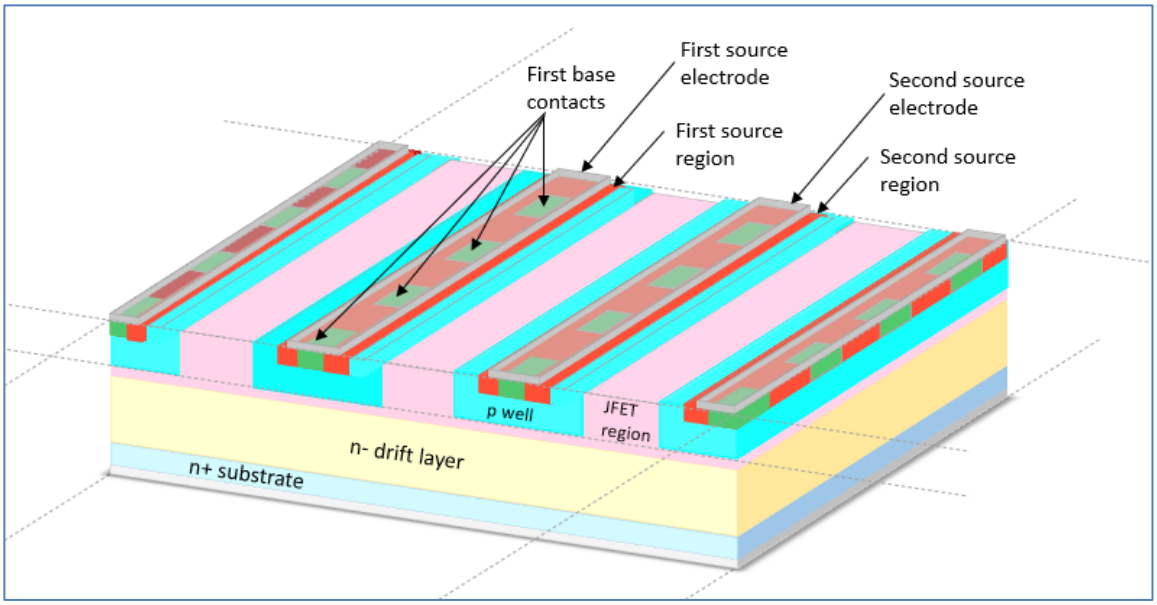
Figure 2A

Id. at Fig. 2A.



Ex. 1010 ¶ 106.

A POSITA would have understood that the source electrode 30 extends into the page with respect to the cross-section image of Figure 2A, and, when modified based on the teachings of Depetro, Ryu's second source electrode would extend along the top of the device over the second source region and define a longitudinal axis consistent with the source electrode of Depetro:



Id. ¶ 107.

i) Limitation 9(i): "a plurality of second base contact regions defined in the first source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode"

Ryu in combination with Depetro discloses limitation 9(i). Ex. 1010 ¶ 108. Ryu teaches a second p+ region 22 implanted into the p-well 20 and positioned in the n+ source region 24. *Id.*; Ex. 1003 at [0045]. The second base contact region is annotated in green in both the unit cell of Figure 2A and the multiple-cell device shown below:

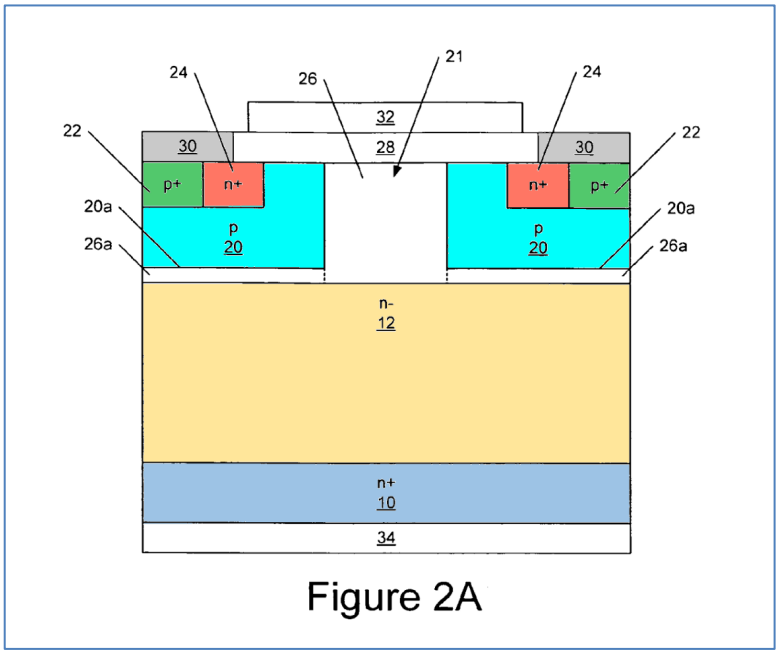
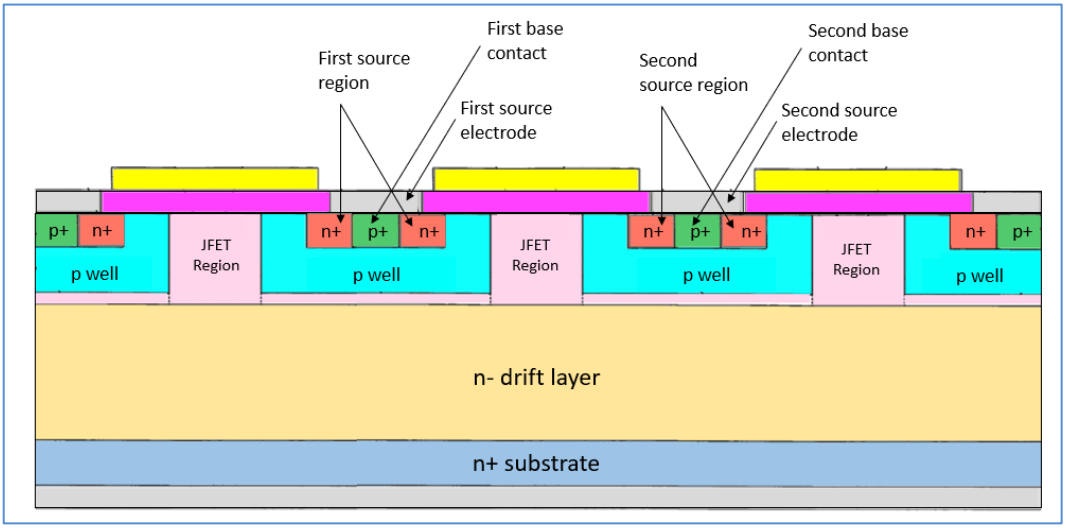


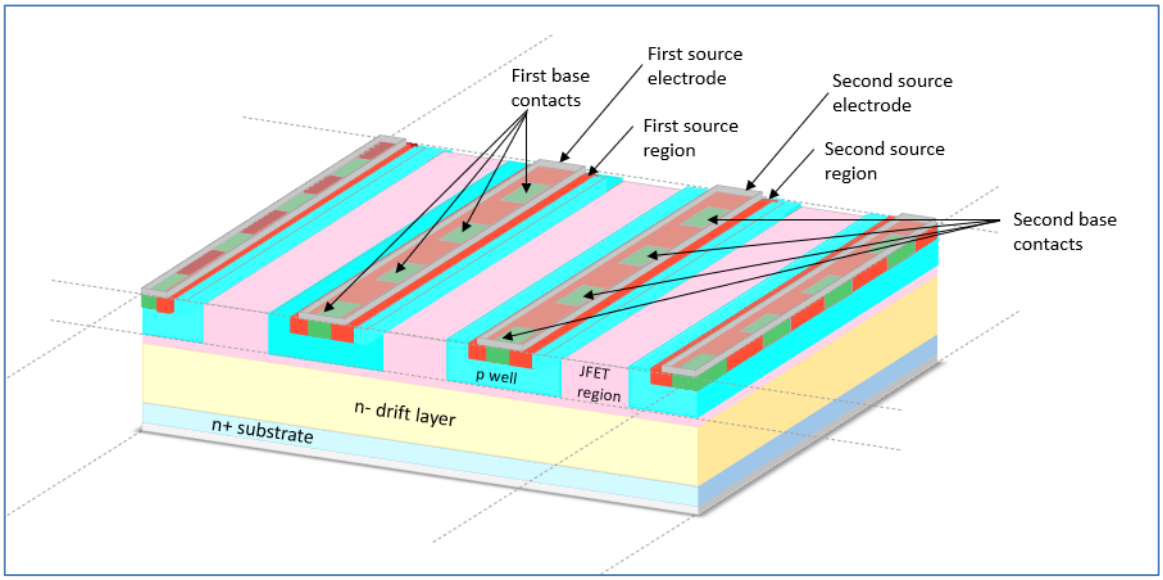
Figure 2A

Id. at Fig. 2A.



Ex. 1010 ¶ 108.

As discussed above, Ryu does not illustrate a top view of the MOSFET, and therefore does not expressly disclose a "plurality" of the second p+ base contact regions 22. *Id*. ¶ 109. Depetro, however, discloses the claimed arrangement of base contact regions. *Id*.; Ex. 1004 at Figs. 1-2. When modified based on the teachings of Depetro, Ryu's p+ base contact regions would be formed as a plurality of islands that are spaced apart from each other in a direction parallel to the longitudinal axis defined by the source electrode:



Ex. 1010 ¶ 109.

j) Limitation 9(j): "a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers"

Ryu discloses limitation 9(j). Ex. 1010 ¶ 110. Ryu teaches that region 21 between the p-wells 20 is a JFET region. Ex. 1003 at [0044]. A POSITA would likewise understand that the region defines a JFET region because it forms depletion zones with the p-wells on either side of it. *Id.* The image below shows the JFET region 21, annotated in pink, positioned between the first and second source regions 24:

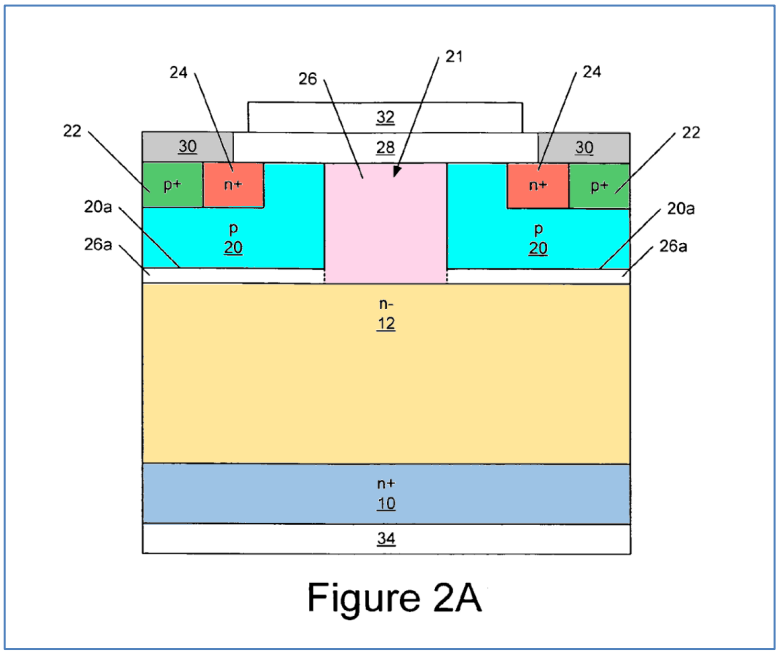


Figure 2A

Id. at Fig. 2A.

Ryu further teaches the JFET region having a width less than about three micrometers. Ex. 1010 ¶¶ 111-112. With respect to Figure 2A, Ryu teaches that if the JFET width is too high, then the electric field in the gate oxide can become too high in the blocking state. *Id*. at [0044]. If the width is too narrow, then the resistance of the JFET region may become very high. *Id*. Thus, Ryu explains that the width utilized for a given device may depend upon the desired blocking voltage and on-state resistance. *Id*.

Ryu addresses these dual concerns by introducing a JFET limiting region below the p-wells of the device. *Id*. at [0039]. The JFET limiting region reduces the depletion zones surrounding the p-wells and thereby reduces the impact of the JFET component of on-resistance. *Id*. This, in turn, allows Ryu to achieve a

smaller JFET width, which provides the benefits of increased cell density, increased blocking voltage, and reduced channel resistance. *Id*. at [0044]; Ex. 1010 ¶ 112. Ryu teaches a preferred width "from about 1 μm to about 10 μm" for the JFET region, which overlaps the claimed range of "less than about three micrometers." *Id*.

The prior art disclosure of an overlapping range meets the claim requirement absent some showing of criticality. *Ineos USA LLC v. Berry Plastics Corp*., 783 F.3d 865, 869-70 (Fed. Cir. 2015) (prior art disclosure of 0.1 to 5% met claim requirement of 0.05 and 0.5%); *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012) (prior art disclosure of "150 ppm or less" met claim requirement of "less than or equal to 50 ppm"). Nothing in the specification of the '633 Patent suggests that the claimed range is critical or achieves unexpected results as compared to the range disclosed in Ryu. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

First, the specification identifies the claimed width as present in only "some embodiments" of the invention; it is not a requirement or critical component of the alleged invention. Ex. 1001 at 6:21-27; 45-50. Indeed, the specification refers to a "shorter width" generically, without specifying any particular dimension that is required to achieve unexpected results. *Id*. Second, the specification states that a shorter width may reduce on-resistance and increase blocking voltage, but neither

result was surprising or unexpected. Ex. 1010 ¶ 114. A POSITA would have understood that a narrower JFET width would yield a shorter pitch between cells, which was known to lower channel resistance component of on-resistance. *Id*. The POSITA also would have understood that a narrower JFET region would yield a higher blocking voltage, as evidenced by Ryu's discussion of this very point. *Id*.; Ex. 1003 at [0044]; Ex. 1015. Accordingly, there is no criticality associated with the claimed JFET width of "less than about three micrometers" as recited in claim 9 or "about one micrometer" as recited in claim 10; the results associated with each range would have been predictable. Ex. 1010 ¶ 114.

Even if there was criticality, a POSITA would have been motivated to adopt the lower end of the JFET width disclosed in Ryu given the known benefits discussed above. *Id*. ¶ 115. In particular, the POSITA would have recognized that the lower end of the range, including widths of 1 to 3 microns, would have provided a smaller cell pitch and therefore lower channel resistance. *Id*. The lower channel resistance would have been balanced against a higher JFET resistance, but Ryu accounts for that consequence by introducing a JFET limiting region. *Id*.; Ex. 1003 at [0039].[8] Additional benefits of the lower end of Ryu's

[8] A POSITA also would have recognized other known techniques for reducing overall on-resistance, including adopting the source-region layouts of Depetro and Choy, which would have counteracted any increase in JFET resistance that would result from adopting a smaller JFET width. Ex. 1010 ¶ 115. Thus, a POSITA

range would have included increased blocking voltage and a higher cell density for the MOSFET, *i.e.*, more current per unit area. *Id.*; Ex. 1010 ¶ 116. And finally, a POSITA would have recognized that the range of widths disclosed in Ryu was a design choice with predictable tradeoffs. *Id.* Thus, JFET widths at the lower end of the range would have been, at a minimum, obvious to try depending on the desired result in terms of on-resistance and blocking voltage. *Id.*

3. Claim 10: "The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer"

The combination of Ryu and Depetro renders obvious claim 10. Ex. 1010 ¶ 117. As discussed in Section XI.A.2, the combination renders obvious claim 9, and Ryu further teaches a JFET width "from about 1 μm to about 10 μm," which overlaps the claimed range of about one micrometer. *Id.* Furthermore, a POSITA would have been motivated to use the lower end of the disclosed range—including a width of about one micrometer—to reduce channel resistance, increase cell density, and increase blocking voltage. *Id.*

4. Claim 11: "The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first

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could achieve the benefits associated with a smaller width, while also achieving a low overall on-resistance. *Id.*

concentration of first type impurities being greater than the second concentration of first type impurities"

The combination of Ryu and Depetro renders obvious claim 11. Ex. 1010 ¶ 118. As discussed in Section XI.A.2, the combination renders obvious claim 9, and Ryu further teaches that both the JFET region 21 and drift layer 12 are doped with n-type impurities, and that the JFET region is more highly doped than the drift layer. Ex. 1003 at [0041]-[0042].

5. Motivation to Combine

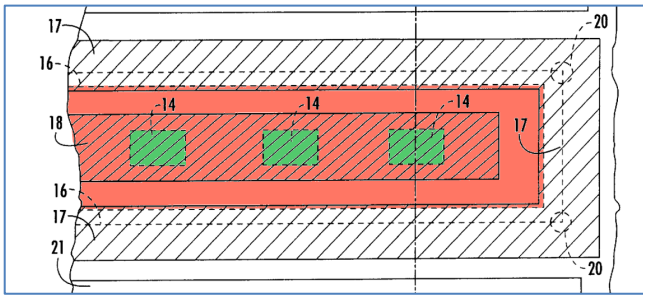
A POSITA would have been motivated to combine the teachings of Ryu and Depetro. Ex. 1010 ¶¶ 119-131.

First, Ryu and Depetro are analogous art to the claimed invention. *Id.* ¶ 120. Both references are in the same field of endeavor as the '633 Patent because they are directed to MOSFETs for high-power applications. *Compare* Ex. 1001 at 1:10-14 *with* Ex. 1003 at [0003]-[0004] *and* Ex. 1004 at 1:10-12. Both references are pertinent to the problems addressed in the '633 Patent: improving the performance of high-power MOSFETs, including through reduced on-resistance and preventing turn-on of the parasitic BJT to avoid premature breakdown. Ex. 1001 at 1:18-36; Ex. 1010 ¶ 120. Accordingly, a POSITA would have looked to the teachings of Ryu and Depetro when considering how to improve the operation of high-power MOSFETs. *Id.*

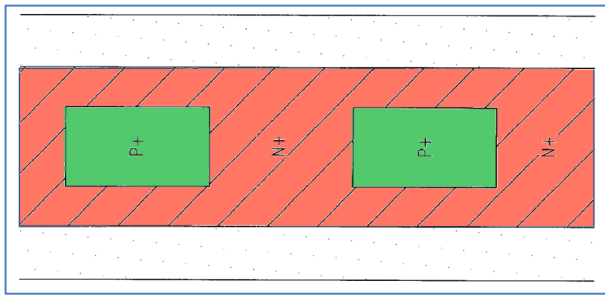
Second, a POSITA would have understood that the teachings of Depetro are directly applicable to the MOSFET of Ryu. *Id*. ¶ 121. Depetro teaches that its device structure and advantages are applicable to vertical double-diffused MOSFETs. Ex. 1004 at 1:9-15; 4:43-48. Ryu explains that its vertical double-implanted MOSFET is a variation of those exact devices. Ex. 1003 at [0006]. When looking to improve the structure and operation of a double-implanted SiC device like Ryu, a POSITA would have looked to known double-diffused silicon devices like Depetro. Ex. 1010 ¶ 121. In particular, he would have looked to designs that were known to improve performance metrics for a power MOSFET. *Id*. This would have led him to references like Depetro, which teaches a source-region layout known to reduce on-resistance while preventing turn on of the parasitic BJT. *Id*.

Third, a POSITA would have had significant motivation to apply the source-region layout of Depetro to the MOSFET of Ryu. *Id*. ¶ 122. As detailed above, Ryu teaches the desirability of low on-resistance for high-power MOSFETs. *Id*. A POSITA would have recognized that reduction of on-resistance could be further improved by adopting a source-region layout like the one disclosed in Depetro, with p+ contacts formed as spaced-apart regions in the n+ source region. *Id*. A POSITA would have understood that the design reduced on-resistance by increasing the effective area of the n+ source regions. *Id*. That understanding is

confirmed by Williams, which teaches the same source-regions layout as Depetro and details its benefits in terms of reduced on-resistance:



Ex. 1004, Depetro at Fig. 1



Ex. 1006, Williams at Fig. 19E

In particular, Williams explains that forming the p+ regions as windows in the n+ source region can maximize the contact area of the n+ region—and therefore reduce on-resistance of the device, without sacrificing suppression of the parasitic BJT, and while achieving alignment of the source region and base contacts. Ex. 1006 at 16:28-35 ("The design can be selected to maximize the N+ source perimeter (to achieve the lowest possible resistance) or to maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device), or to compromise between the two."); 17:15-19. A POSITA would recognize that the same benefit results from the design of Depetro, which, like Williams, forms the p+ contacts as windows in the n+ source region.

Ex. 1010 ¶ 123. Applying that design to Ryu would further its goal of reducing on-resistance of the device. *Id*.[9]

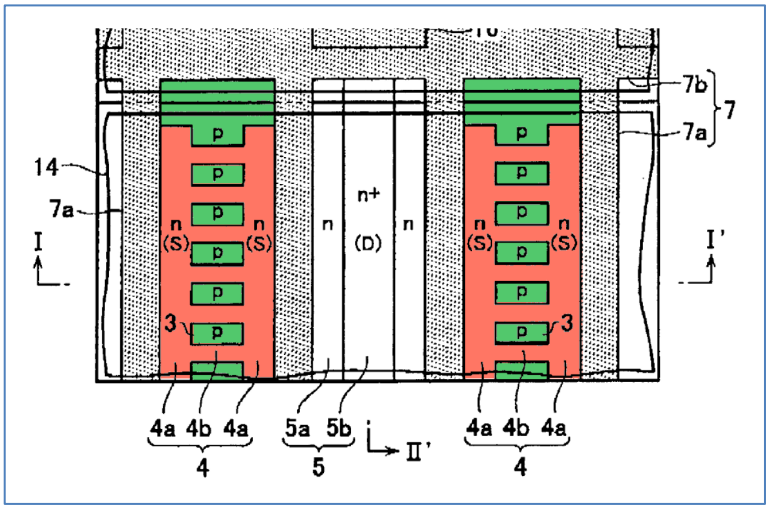
A POSITA also would have been motivated to form Ryu's source contact 30 as a longitudinal stripe consistent with the source electrode 18 in Depetro. *Id*. ¶ 125. After implanting Ryu's p+ base contacts as spaced apart regions, the POSITA would have been motivated to short the contacts to the n+ source region in order to prevent unwanted turn-on of the parasitic BJT. *Id*. The most straight-forward manner in which to accomplish this—and the technique taught by Depetro—would have been to form an ohmic contact as a stripe over the source region and in contact with each p+ contact. *Id*. Ryu was readily adaptable to this design because it disclosed a source contact 30 shorting the source region and p+ base contact. *Id*.; Ex. 1003 at Fig. 2A.

Fourth, a POSITA would have recognized that the source-region layout of Depetro would improve the operation of *SiC* devices like Ryu. *Id*. ¶ 126. In the

[9] As explained in Williams, the tradeoff for increasing the effective area of the n+ source region is a reduction in ruggedness of the device. Ex. 1006 at 16:28-35. That tradeoff would not dissuade a POSITA from adopting spaced apart p+ regions, because he or she would have recognized that the design can be balanced by adjusting the size and doping concentration of the p+ regions. *Id*.; Ex. 1010 ¶ 124. Furthermore, Depetro accounts for the potential reduction in ruggedness by introducing a strongly doped p+ region at the edge of the body. Ex. 1004 at 3:45-54. A POSITA would have understood that similar considerations could be applied to Ryu in order to achieve the benefit of reduced on-resistance without compromising ruggedness.

late 1990s and early 2000s, SiC devices emerged as a next-generation technology for high-power MOSFETs. *Id*. To that end, it was known that SiC devices had to achieve low on-resistance while still suppressing turn-on of the parasitic BJT and maintaining a high blocking voltage. *Id*. Thus, those in the art looked to design techniques to achieve those goals. *Id*. The techniques would have included designing the layout of the n+ source region and p+ base contact regions to increase the effective area of the source region while maintaining sufficient body contact, exactly as disclosed in Depetro and Williams. *Id*.

The prior art confirms this understanding. Ex. 1010 ¶ 127. Nakayama teaches a power MOSFET designed to achieve low on-resistance and enhanced switching performance. Ex. 1005 at [0005]. Embodiments of the MOSFET use the same source-region geometry as Depetro, with p-type contact regions spaced apart in the n-type source regions:



Id. at Fig. 11.

Nakayama teaches that these embodiments improve on-resistance without impacting switching performance. *Id*. at [0057] ("[B]y forming the source layer 4 into a ladder-like planar pattern to suppress or minimize an increase in lateral-directional resistance of the base layer 3 while at the same time permitting the stripe portions 4 a of source layer 4 to stay smaller in width. Thus, it is possible to achieve high-reliability electrical contact of the short electrode 9 with the source layer 4 while retaining enhanced avalanche ratings."). Nakayama also teaches that the design is applicable in both silicon and SiC devices. *Id*. at [0045].

In view of these teachings, a POSITA would have understood the benefits of Depetro's source-region layout for silicon devices would apply to SiC devices like the MOSFET of Ryu. Ex. 1010 ¶ 129. Indeed, Ryu recognizes that its double-implanted device is a "variation" of silicon double-diffused devices like Depetro. Ex. 1003 at [0006]. This provides additional rationale to combine their teachings. *Id*.; *KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1731 (2007).

Fifth, a POSITA would have understood there were a finite number of known design choices for the source-region layout of a device like Ryu. Ex. 1010 ¶ 130. Known designs for the arrangement of p-type material in an n-type source region included hexagonal cells, square cells, stripes, alternating strips, and islands that are either connected or spaced-apart. *Id*.; Ex. 1006 at Figs. 4A, 4B, 19A-F. The tradeoffs associated with each design choice were also well known. As

Williams explains, the "design can be selected to maximize the N+ source perimeter (to achieve the lowest possible resistance) or to maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device), or to compromise between the two." Ex. 1006 at 16:28-35. Nakayama likewise teaches reduction of on-resistance for spaced-apart p-type sections as compared to a linear-strip of p-type material. Ex. 1005 at Figs. 1, 11. Accordingly, because the claimed design was among a finite number of known layout choices—with predictable performance results—it would have been obvious to try when implementing the MOSFET of Ryu. *KSR*, 127 U.S. at 1732.

6. Reasonable Expectation of Success

A POSITA also would have had a reasonable expectation of success in combining the teachings of Ryu and Depetro to achieve the claimed invention. Ex. 1010 ¶¶ 132-139.

First, a POSITA would have been familiar with different source-region layouts and capable of implementing them with a reasonable expectation of success. *Id*. ¶ 133. This is particularly true with respect to the source-region layout of Depetro, which was taught in both silicon and SiC devices. *Id*.; Ex. 1006 at Figs. 19E-F; Ex. 1005 at Fig. 4. Techniques for implanting p+ regions in a spaced-apart arrangement within an n+ source region were well known and predictable in the field, including using masks to selectively implant the respective

regions. Ex. 1004 at 4:1-9, 29-33; Ex. 1006 at Abstract; Ex. 1010 ¶ 133. Indeed, Nakayama teaches that an n-type source region with spaced-apart p-type base contacts was applicable to SiC devices. *Id.*; Ex. 1007 at [0045], [0057]. Thus, a POSITA would have reasonably expected the design to work when implemented in the SiC device of Ryu. Ex. 1010 ¶ 133.

Second, a POSITA would have understood that techniques for adapting silicon designs to SiC were well known and predictable. *Id.* ¶¶ 134-135. A key difference between the technologies was that silicon allowed for diffusion of n-type and p-type impurities, whereas SiC relied on implantation. *Id.* By the time of the alleged invention, SiC technology had developed significantly and techniques to implant n+ source regions with spaced-apart p+ contacts—as disclosed in Depetro—were routine. *Id.*; *see also* Section VI.E. Relying on known techniques, a POSITA would have had a reasonable expectation of success in achieving a MOSFET device that combines the teachings of Ryu and Depetro discussed above. Ex. 1010 ¶¶ 134-135.

Third, Ryu teaches that its SiC device is a variation of prior silicon devices. Ex. 1003 at [0006]. Thus, a POSITA would have reasonably expected that Ryu's device could be adapted to known silicon designs—such as the source-region layout of Depetro—with predictable results. Ex. 1010 ¶ 136. Indeed, the device in Figure 2A of Ryu already includes p+ body contacts within the n+ source regions

and an overlying ohmic contact. Ex. 1003 at Fig. 2A, [0044]-[0047]. Thus, the device would not require modification of its layers and structures in order to adopt the source-region and base contact structure of Depetro. Ex. 1010 ¶ 136. Indeed, a POSITA would have recognized that the resulting device would retain the same cross-section as shown in Figure 2A of Ryu. *Id*.

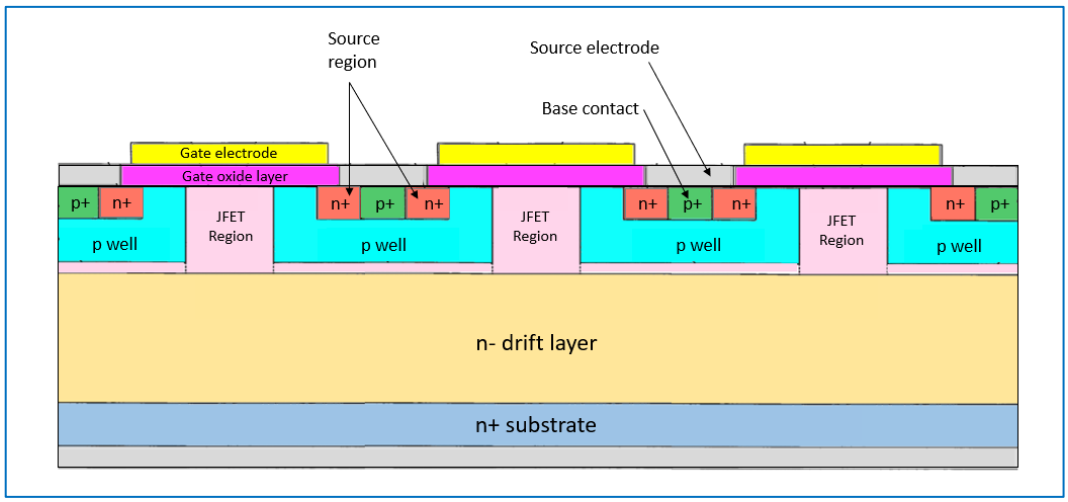
Fourth, the topside source-region and base-contact structure of Depetro is applicable to vertical MOSFETs. Ex. 1004 at 4:44-50. Thus, a POSITA would have expected the source-region and base-contact structure to apply predictably to the vertical MOSFET of Ryu. Ex. 1010 ¶ 137.

Finally, during prosecution of the application underlying the '633 Patent, the Applicant identified purported difficulties in achieving the claimed invention. Ex. 1002 at 74-78. Those difficulties, however, focused on forming the claimed JFET region on a silicon-carbide substrate; they had nothing to do with the source-region layout of the device or the formation of p+ contacts in the n+ source regions. *Id*. Ryu already teaches the claimed JFET region formed on a SiC substrate. Ex. 1003 at [0044]-[0047]. Modifying the source-region layout of the device would not impact the design of those structures. Ex. 1010 ¶ 138.

B. Ground 2: Ryu and Choy Render Obvious Claims 9-11

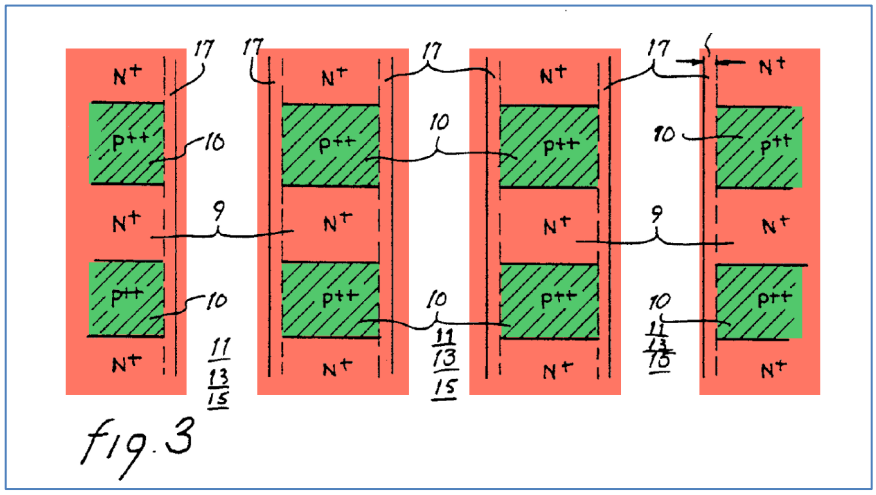
1. Overview

The combined teachings of Ryu and Choy render obvious claims 9-11. Ex. 1010 ¶¶ 140-174. Ryu teaches a vertical double-implanted MOSFET with a cross-sectional structure that includes the regions specified in claims 9-11 as illustrated in the demonstrative below:



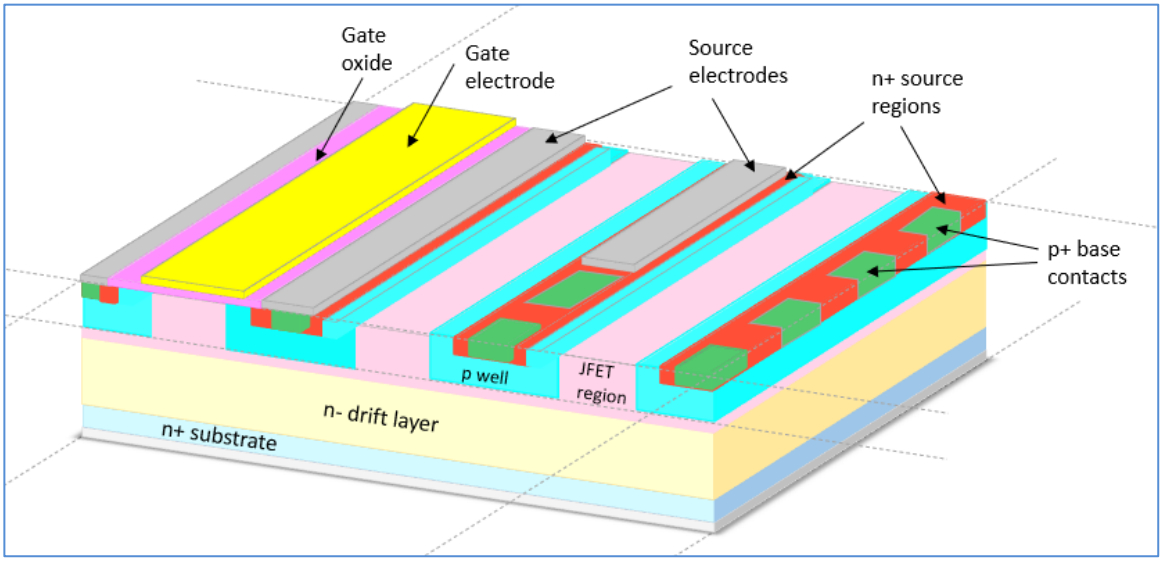
Id.; Ex. 1003 at Fig. 2A.

Choy teaches a double-implanted vertical MOSFET that includes a plurality of p-type base contacts spaced-apart in an n-type source region:



Ex. 1005 at Fig. 3.

When the source-region layout of Choy is applied to the MOSFET of Ryu, the resulting structure includes each element of challenged claims 9-11. In particular, the p+ base contacts 22 of Ryu would be formed in the n+ source region 24 as a plurality of spaced-apart islands defined along the longitudinal axis of the source electrode 30:



Ex. 1010 ¶ 142.

A POSITA would have been motivated to combine the teachings of Ryu and Choy because it would have reduced the on-resistance of the resulting device, while preventing unwanted turn-on of the parasitic BJT and maintaining a high blocking voltage. *Id*. ¶ 143. The combination of Ryu and Choy is detailed in the following sections. The teachings of the references are addressed in Sections XI.B.2-4. Motivation to combine and reasonable expectation of success are addressed in Sections XI.B.5-6.

2. Claim 9

a) Limitation 9(a): "A double-implanted metal-oxide semiconductor field-effect transistor"

Ryu discloses limitation 9(a). *See* Section XI.A.2(a); Ex. 1010 ¶ 144.

b) Limitation 9(b): "a silicon-carbide substrate"

Ryu discloses limitation 9(b). *See* Section XI.A.2(b); Ex. 1010 ¶ 145. The silicon-carbide substrate is shown in blue below:

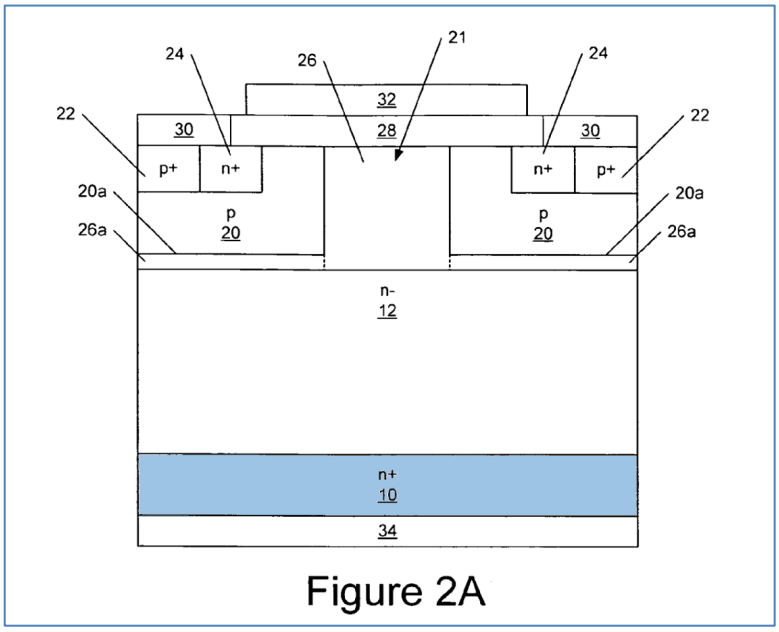


Figure 2A

Ex. 1003 at Fig. 2A.

c) Limitation 9(c): "a drift semiconductor layer formed on a front side of the semiconductor substrate"

Ryu discloses limitation 9(c). *See* Section XI.A.2(c); Ex. 1010 ¶ 146. The drift layer is shown in tan below:

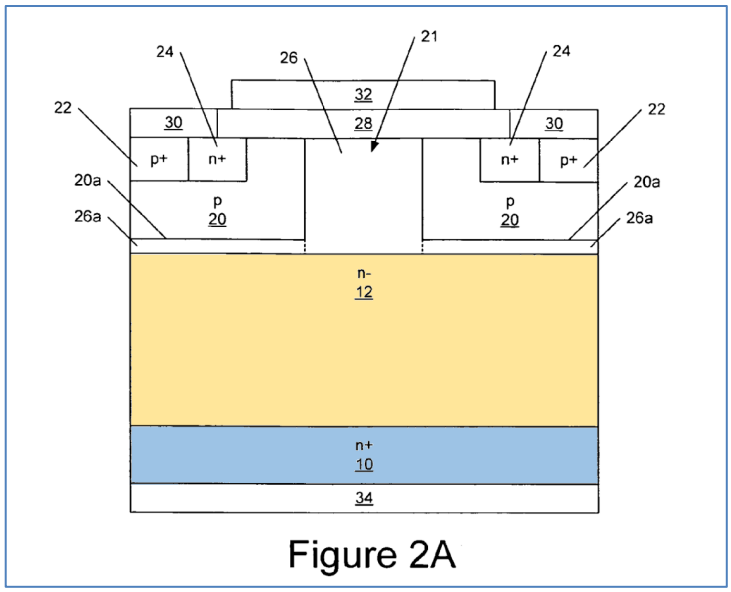


Figure 2A

Ex. 1003 at Fig. 2A.

d) Limitation 9(d): "a first source region"

Ryu discloses limitation 9(d). *See* Section XI.A.2(d) *supra*. The first source region is shown in red in the images below:

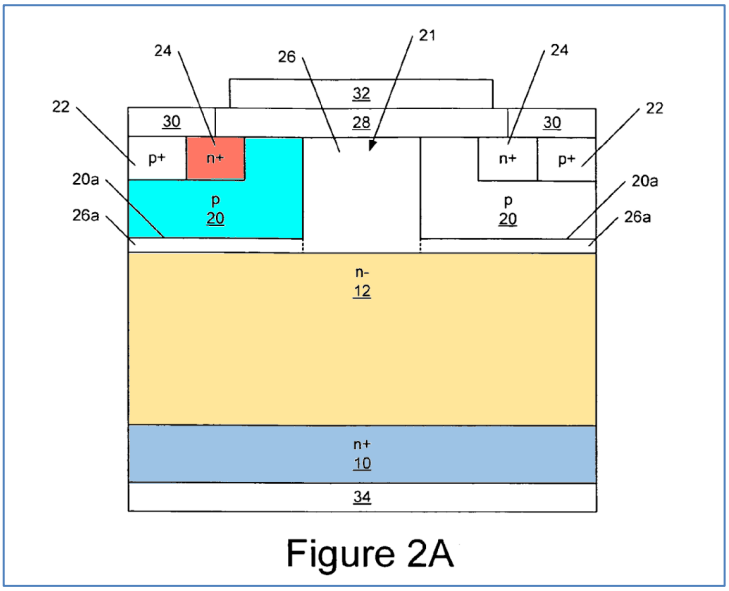
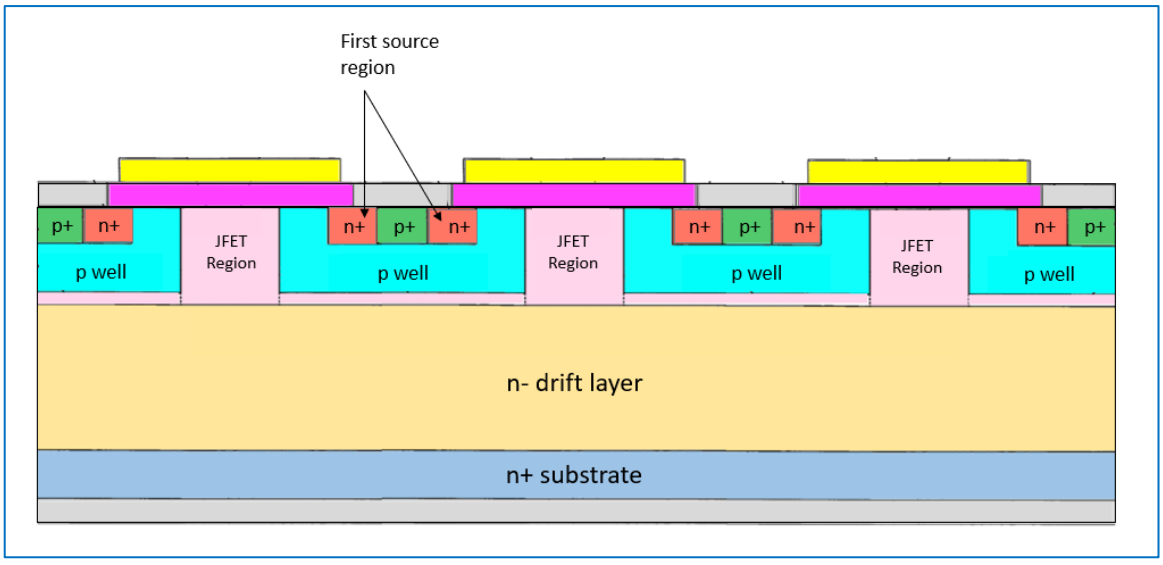


Figure 2A

Ex. 1003 at Fig. 2A.



Ex. 1010 ¶ 147.

e) Limitation 9(e): a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis"

Ryu in combination with Choy discloses limitation 9(e). Ex. 1010 ¶ 148. Ryu discloses a source contact 30 formed over the n+ source region 24 and p+ base contacts 22 to form an ohmic contact that shorts the two regions. Ex. 1003 at [0047]. The first source electrode is annotated in gray in both the unit cell of Figure 2A and the multiple-cell device in the demonstrative below:

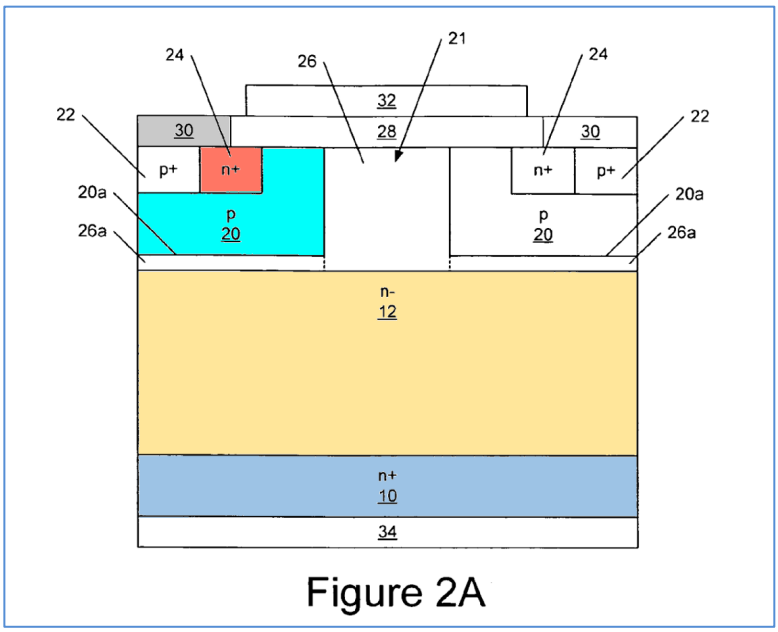
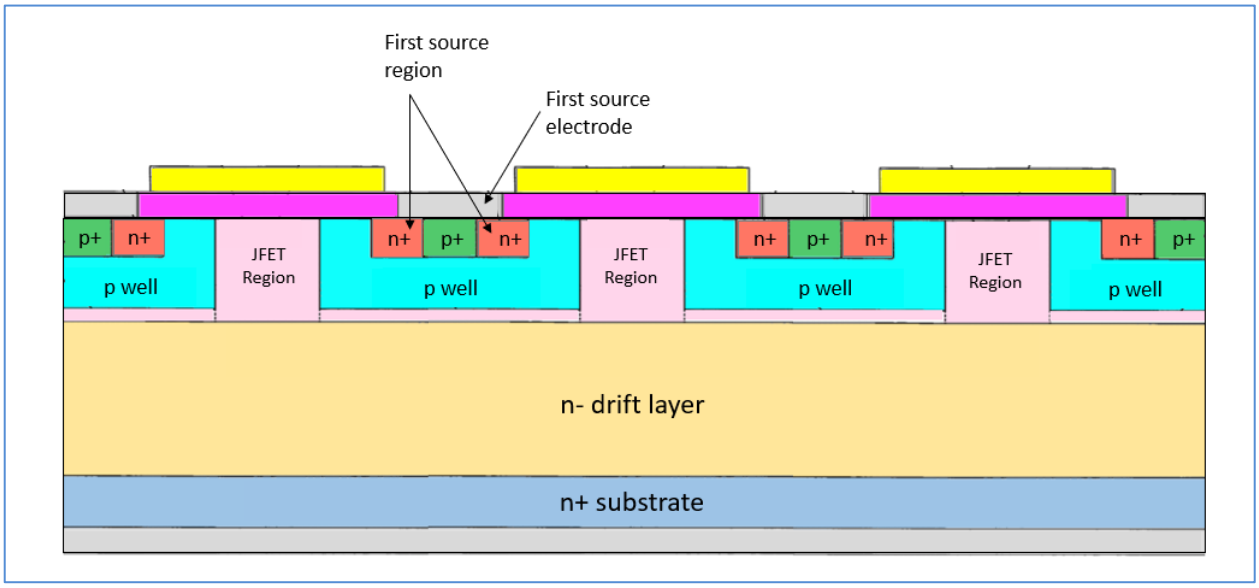


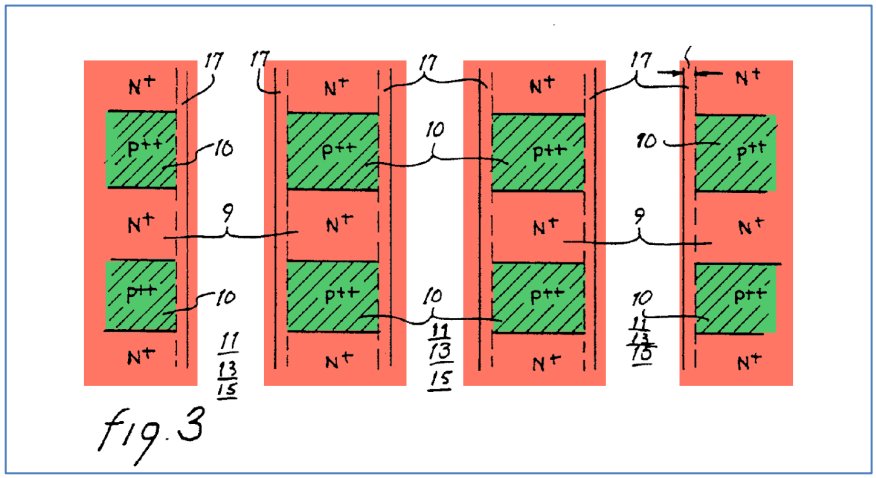
Figure 2A

Ex. 1003 at Fig. 2A.



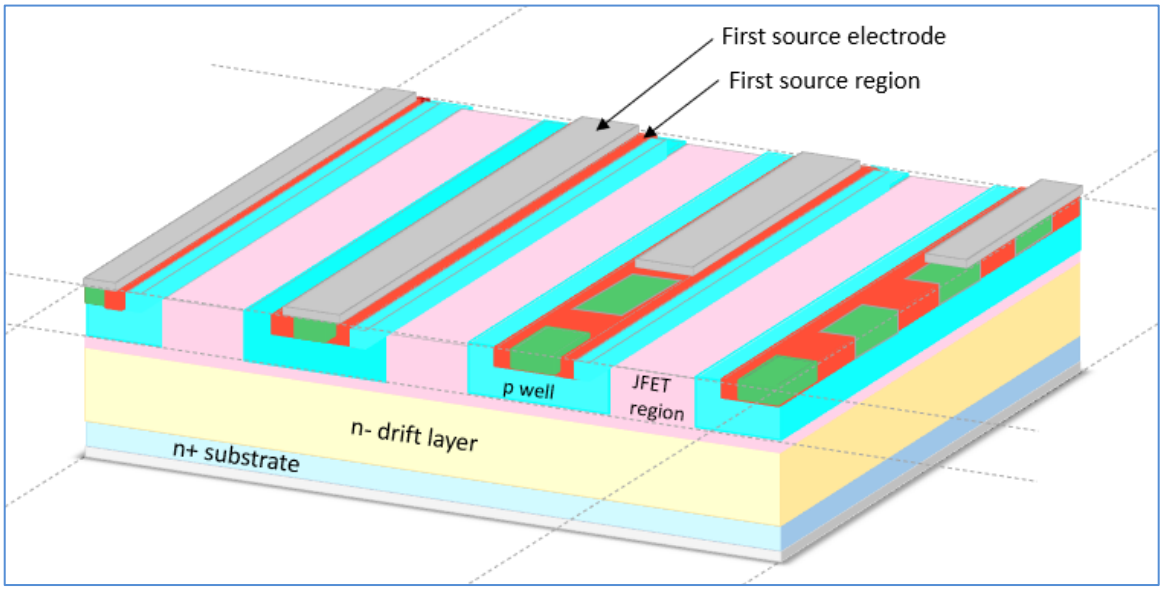
Ex. 1010 ¶ 148.

A POSITA would have understood that the source contact 30 extends into the page with respect to the cross-section image of Figure 2A. *Id.* ¶ 149. They also would have understood that, when the source-region layout of Choy is applied to the device of Ryu, the source contact 30 would define a longitudinal axis into the page. *Id.* The source-region layout of Choy is illustrated in the image below. *Id.* It includes an n-type source region with p-type base contacts spaced apart along a longitudinal axis:



Id. at Fig. 3

Choy further teaches that the n-type source region and p-type base contacts are shorted by metallization formed within each stripe of Figure 3. *Id*. at 3:32-40 ("Following conventional metal deposition and definition, these regions will be electrically shorted to each other in each stripe."). Applying that teaching to Ryu, a POSITA would have formed the source contact as a strip defining a longitudinal axis that shorts the n+ source region to the p+ base contacts within each strip. Ex. 1010 ¶ 150. The resulting device would thus meet the requirements of limitation 9(e) as shown in the demonstrative below:



Id.

f) Limitation 9(f): "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode"

Ryu in combination with Choy discloses limitation 9(f). Ex. 1010 ¶¶ 151-152. Ryu teaches a first p+ base contact region 22 implanted into the p-well 20 and positioned in the n+ source region 24, illustrated in green in the image and demonstrative below:

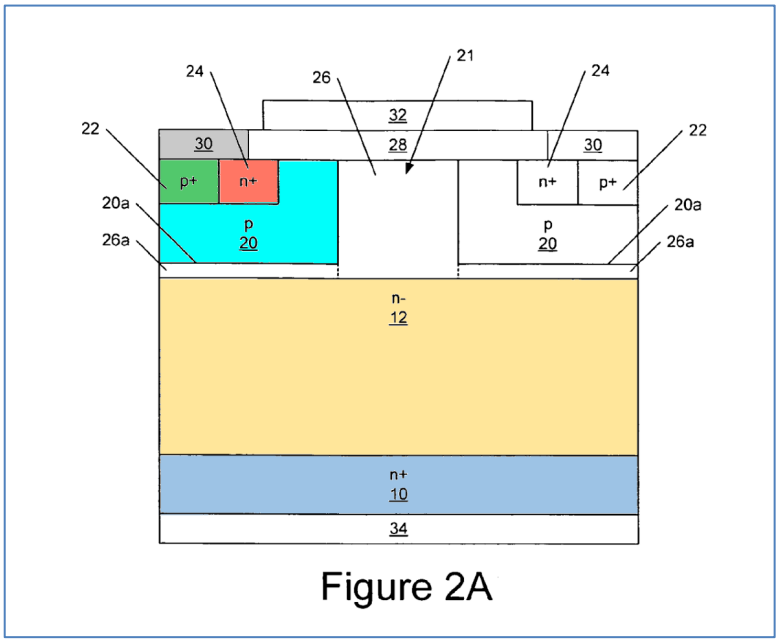
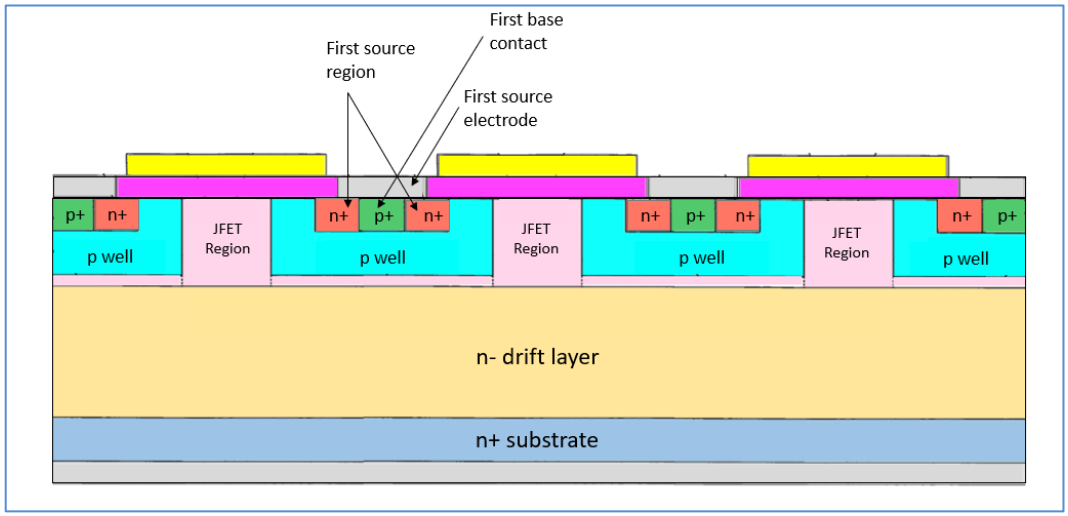


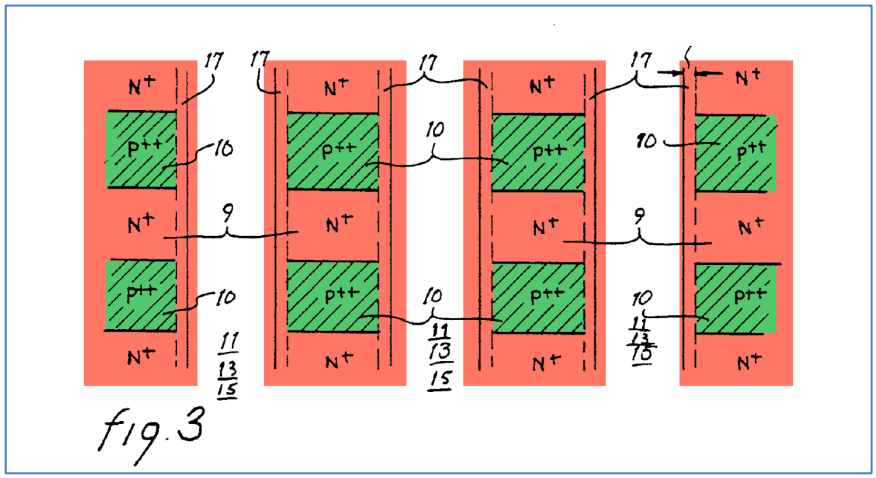
Figure 2A

Ex. 1003 at Fig. 2A.



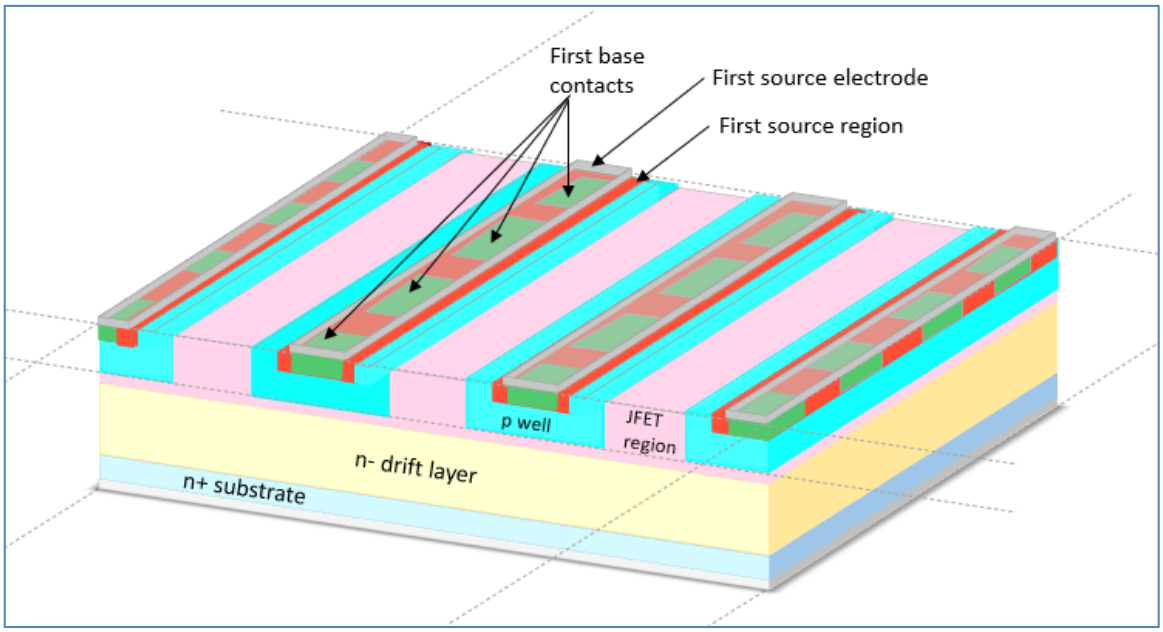
Ex. 1010 ¶ 151.

Choy teaches a plurality of p-type base contact regions 10 defined in source region 9 and spaced apart along a longitudinal axis defined by source metallization:



Id. at Fig. 3; 3:32-40.

When modified based on the teachings of Choy, Ryu's p+ base contact regions 22 would be formed as a plurality of regions that are spaced apart from each other in a direction parallel to the longitudinal axis defined by the source electrode 30 as shown in the demonstrative below:



Ex. 1010 ¶ 152.

g) Limitation 9(g): "a second source region"

Ryu discloses limitation 9(g). *See* Section XI.A.2(g). The second source region is shown in red in the images below:

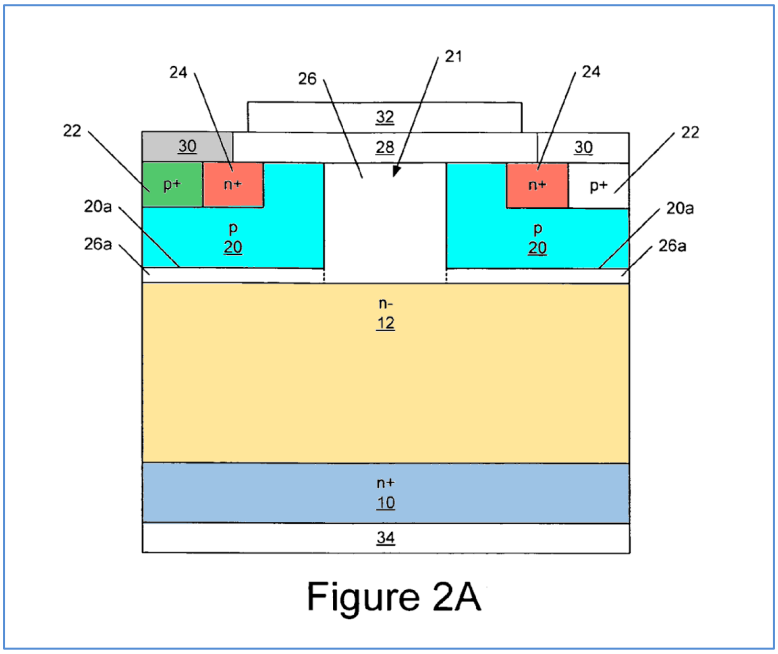
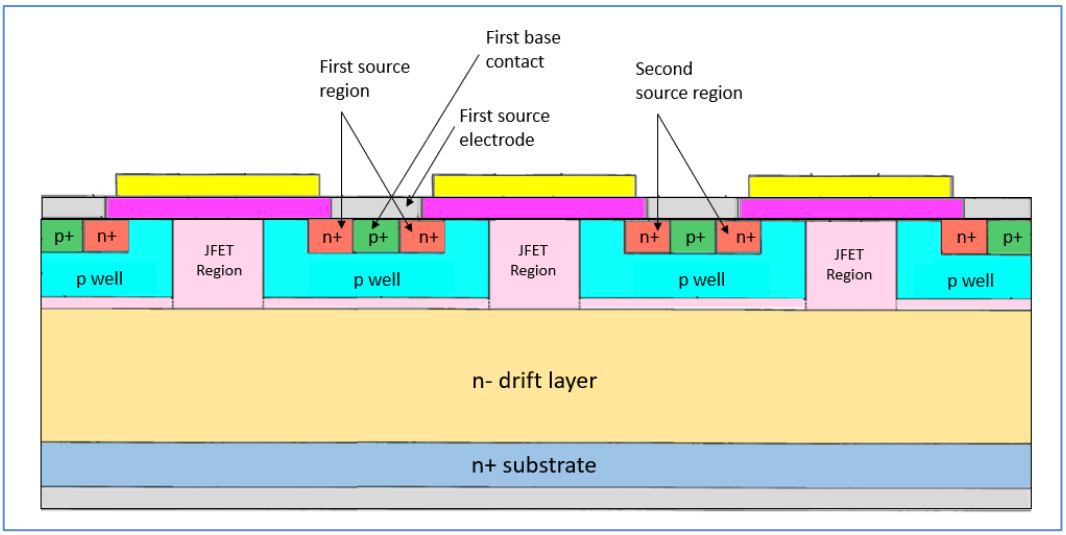


Figure 2A

Ex. 1003 at Fig. 2A.



Ex. 1010 ¶ 154.

h) Limitation 9(h): "a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis"

Ryu in combination with Choy discloses limitation 9(h). Section XI.A.2(h).

Ryu teaches a second source electrode 30 formed over the n+ source region 24 and p+ base contacts 22 as shown in the image and demonstrative below:

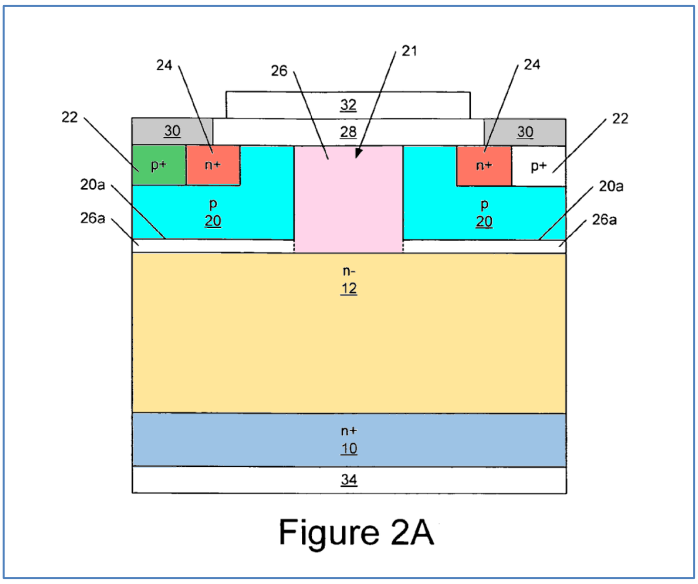
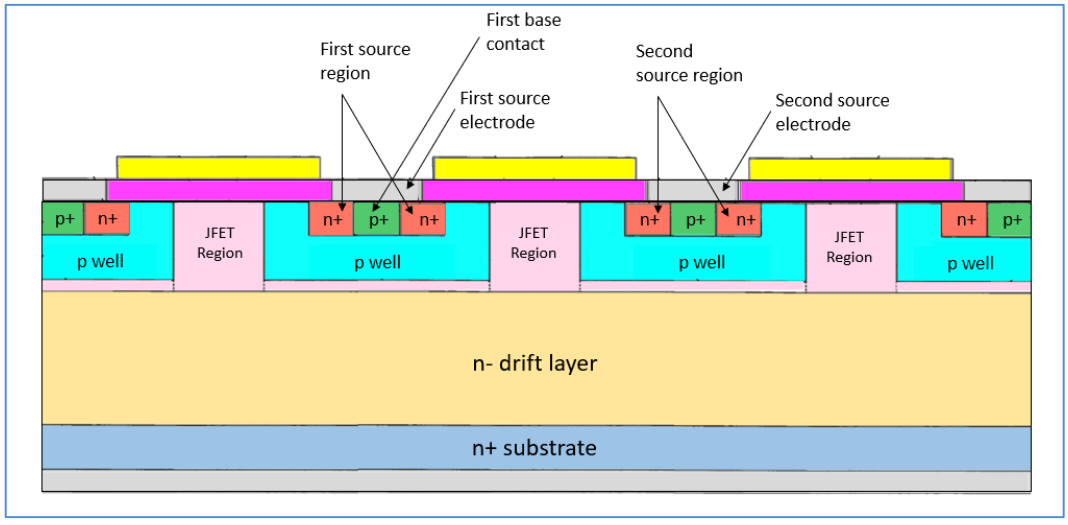


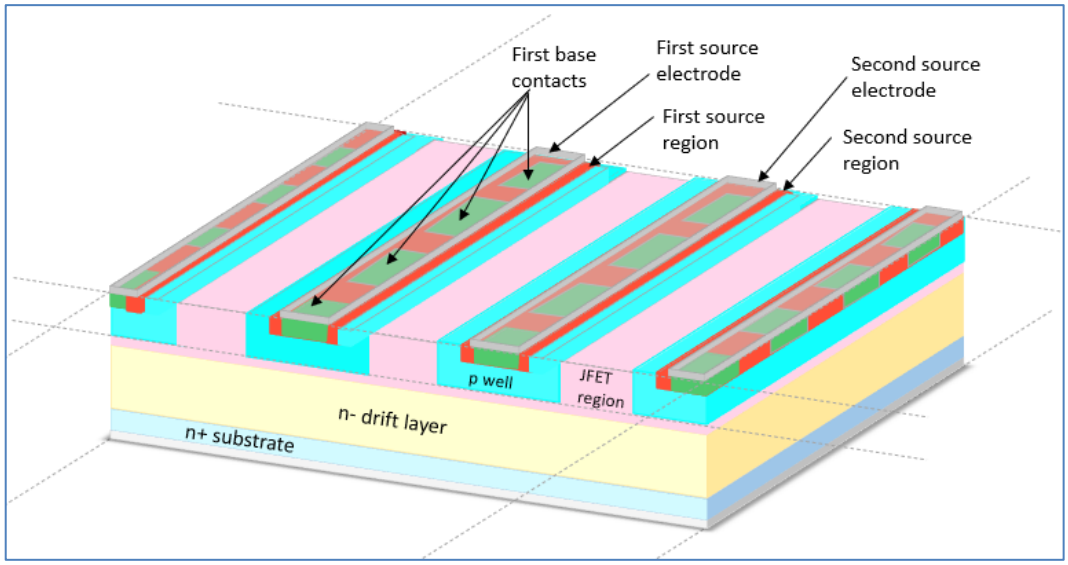
Figure 2A

Ex. 1003 at Fig. 2A.



Ex. 1010 ¶ 155.

When the source-region layout of Choy is applied to the device of Ryu, the second source electrode would define a longitudinal axis that extends along the top of the device and over the second source region as shown below:



Id. ¶ 156; Ex. 1005 at 3:32-40.

i) Limitation 9(i): "a plurality of second base contact regions defined in the first source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode"

Ryu in combination with Choy discloses limitation 9(i). Ex. 1010 ¶¶ 157-158. Ryu teaches a second p+ base contact region 22 implanted into the p-well 20 and positioned in the n+ source region 24 as shown in the image and demonstrative below:

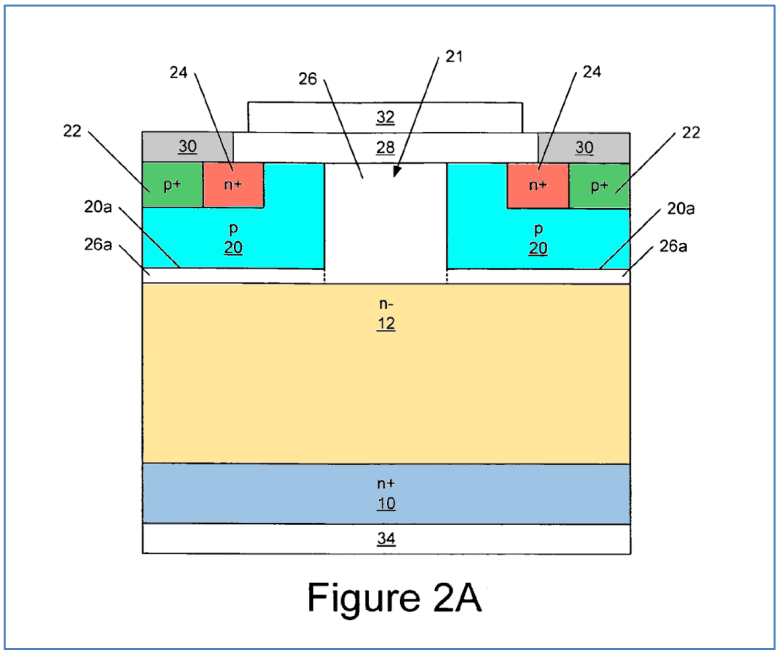
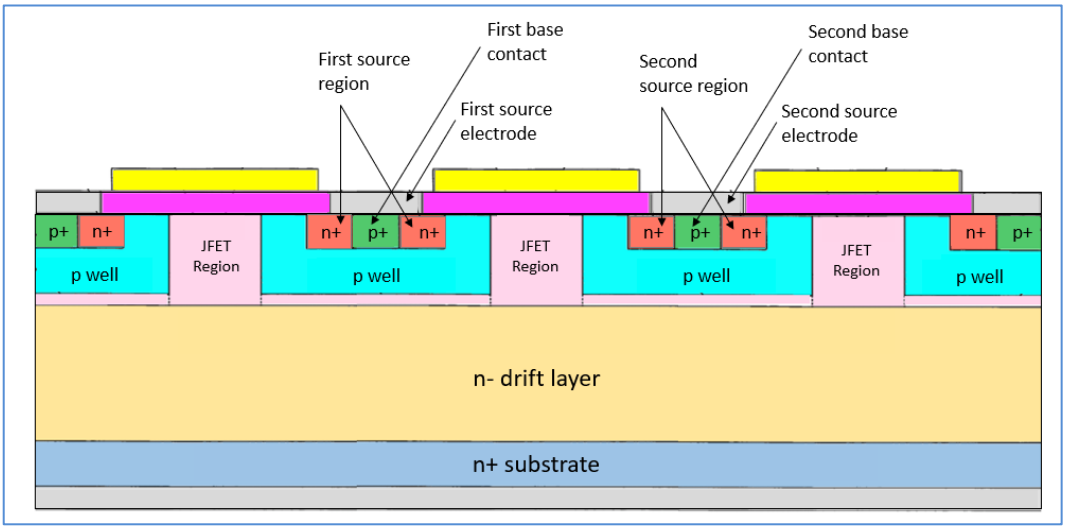


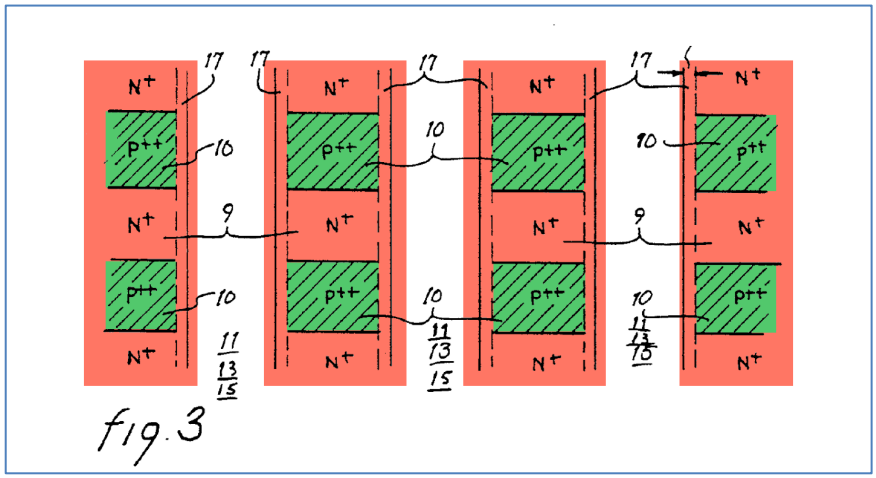
Figure 2A

Id. at Fig. 2A.



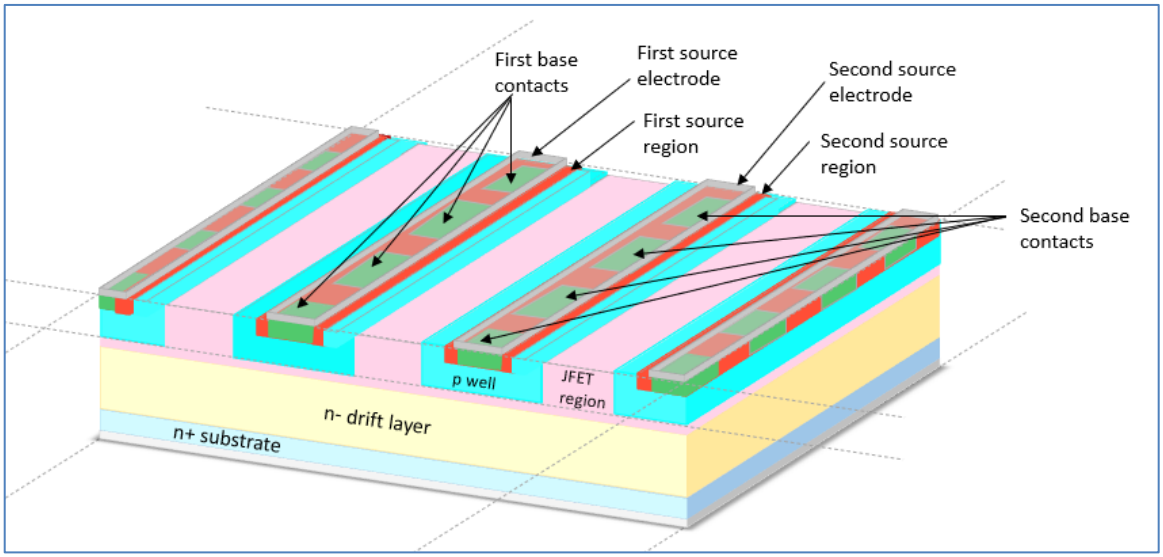
Ex. 1010 ¶ 157.

Choy teaches a plurality of second base contact regions 10 defined in source region 9 and spaced apart along the longitudinal axis defined by source metal:



Ex. 1005 at Fig. 3; 3:32-40.

When modified based on the teachings of Choy, Ryu's p+ base contact regions 22 would be formed as a plurality of regions that are spaced apart from each other in a direction parallel to the longitudinal axis defined by the source electrode 30 as shown below:



Ex. 1010 ¶ 159.

j) Limitation 9(j): "a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers"

Ryu teaches and renders obvious limitation 9(j). *See* Section XI.A.2(j); Ex. 1010 ¶¶ 110-116, 160.

3. Claim 10: "The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer"

The combination of Ryu and Choy renders obvious claim 10. Ex. 1010 ¶ 110-116, 161. As discussed in Section XI.B.2, the combination renders obvious claim 9, and Ryu teaches the additional requirements of claim 10. *Id*.

4. Claim 11: "The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities"

The combination of Ryu and Choy renders obvious claim 11. Ex. 1010 ¶ 110-116, 162. As discussed in Section XI.B.2, the combination renders obvious claim 9, and Ryu teaches the additional requirements of claim 11. *Id*.

5. Motivation to Combine

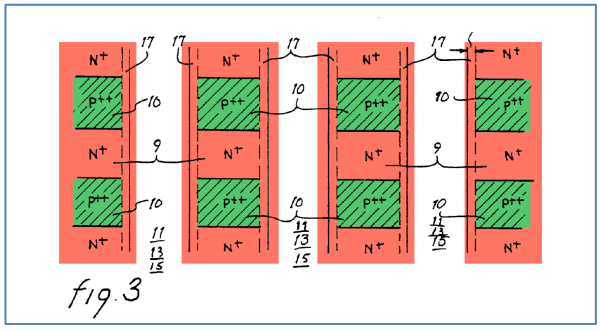
A POSITA would have been motivated to combine the teachings of Ryu and Choy. Ex. 1010 ¶¶ 163-169.

First, Ryu and Choy are analogous art to the claimed invention. *Id*. at ¶ 164. Both references are in the same field of endeavor as the '633 Patent because they are directed to vertical MOSFETs for high-power applications. *Compare* Ex. 1001 at 1:10-14 *with* Ex. 1005 at 1:5-39. Both references are pertinent to the problems addressed in the '633 Patent: improving the performance of high-power devices, including through reduced on-resistance and preventing turn-on of the parasitic BJT. Ex. 1001 at 1:18-36; Ex. 1005 at 3:3-16. Accordingly, a POSITA would have looked to the teachings of Ryu and Choy when considering how to improve the operation of high-power MOSFETs.

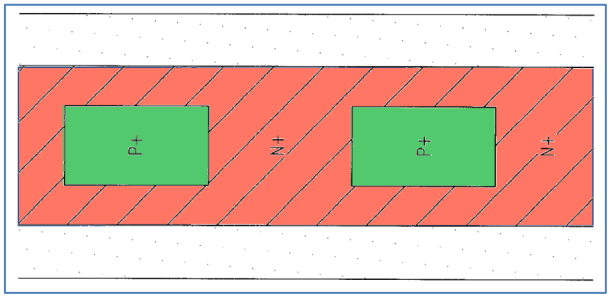
Second, a POSITA would have understood that the teachings of Choy are directly applicable to the device of Ryu. Both references teach vertical power MOSFETs formed using a double-implantation procedures. Ex. 1003 at [0006]-[0009]; Ex. 1005 at 2:31-53, 3:3-23. When looking to improve the structure and operation of the device of Ryu, he would have looked to known double-implanted devices. Ex. 1010 ¶ 165. In particular, he would have looked to designs that were known to improve performance metrics for a power MOSFET. *Id*. This would have led him to references like Choy, which teaches a source-region layout known to reduce on-resistance while preventing turn on of the parasitic BJT. *Id*.

Third, a POSITA would have had significant motivation to apply the source-region layout of Choy to the MOSFET of Ryu. *Id*. ¶ 166. As detailed above, Ryu

teaches the desirability of low on-resistance for high-power MOSFETs. *Id.* A POSITA would have recognized that reduction of on-resistance could be further improved by adopting a source-region layout like the one disclosed in Choy, with p+ contacts formed as spaced-apart regions in the n+ source region. *Id.* A POSITA would have understood that the design reduced on-resistance by increasing the effective area of the n+ source regions. *Id.* That understanding is confirmed by Williams, which teaches the same source-regions layout as Choy and details its benefits in terms of reduced on-resistance:



Ex. 1005, Choy at Fig. 3



Ex. 1006, Williams at Fig. 19E

Williams explains that forming the p+ regions as windows in the n+ source region can maximize the contact area of the n+ region—and therefore reduce on-resistance of the device—without sacrificing suppression of the parasitic bipolar transistor. Ex. 1006 at 16:28-35; 17:15-19. A POSITA would have recognized that the same benefit resulted from the design of Choy, which, like Williams, forms the p+ contacts as windows in the n+ source region. Ex. 1010 ¶ 166. Applying that design to Ryu would further its goal of reducing on-resistance. *Id.*

Fourth, a POSITA would have recognized that the source-region layout of Choy would improve the operation of SiC devices like Ryu. *Id*. ¶ 168. As detailed above, the Nakayama reference teaches a source-region layout similar to Choy, with spaced-apart p-type base contacts. Ex. 1005 at Fig. 11. Nakayama teaches that the source-region layout reduces on resistance and is applicable in silicon carbide. *Id*. at [0045], [0057]. In view of these teachings, a POSITA would have appreciated that Choy's similar source-region layout would provide the same benefit to Ryu's SiC device. Ex. 1010 ¶ 168. *KSR*, 550 U.S. at 1731.

Fifth, a POSITA would have understood there were a finite number of known design choices for the source-regions layout of a device like Ryu, one of which was the spaced-apart p-type regions as disclosed in Choy. Ex. 1010 ¶ 169. Thus, Choy was among a finite number of known layout choices—with predictable performance results—and would have been obvious to try when implementing the MOSFET of Ryu. *KSR*, 550 U.S. at 1732.

6. Reasonable Expectation of Success

A POSITA likewise would have had a reasonable expectation of success in combining the teachings of Ryu and Choy to achieve the claimed invention. Ex. 1010 ¶¶ 133-137, 170-174.

First, a POSITA would have been familiar with different source-region layouts and capable of implementing them in known MOSFET structures with a reasonable expectation of success. *Id*. ¶¶ 133, 171.

Second, a POSITA would have understood that techniques for adapting known MOSFET source region designs to SiC were well known and predictable. *Id*. ¶¶ 134-135, 172.

Third, Ryu teaches that its SiC device is a variation of prior MOSFETs devices. Ex. 1003 at [0006]. Thus, a POSITA would have reasonably expected that Ryu's device could be adapted to known designs—such as the source-region layout of Choy—with predictable results. Ex. 1010 ¶¶ 136, 173. Indeed, both Ryu and Choy teach double-implanted MOSFETs with similar cross-sections, and the device in Fig. 2A of Ryu already includes p+ body contacts within the n+ source regions and an overlying ohmic contact. Ex. 1003 at Fig. 2A, [0044]-[0047]. Thus, the device would not require modification of its layers, structures, or general fabrication technique in order to adopt the source-region layout of Choy. Ex. 1010 ¶ 173.

Finally, the proposed modification would not implicate any of the alleged difficulties identified by the Applicant during prosecution. Ex. 1010 ¶¶ 137, 174.

C. Secondary Considerations

Wolfspeed is not aware of any evidence regarding secondary considerations of non-obviousness, and Purdue did not identify any such evidence in the patent specification, prosecution history, or related district court complaint. Exs. 1001, 1002, 1016; Ex. 1010 ¶ 175. To the extent Purdue attempts to identify evidence of secondary considerations at a later point in the proceeding, Wolfspeed reserves the right to address it at that time.

XII. DISCRETIONARY FACTORS

A. 35 U.S.C. § 314

The *General Plastic* factors weigh against denial of this Petition. *General Plastic Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, slip op. at 9-10 (Sept. 6, 2017) (*precedential*).

Regarding Factor 1, Wolfspeed has not previously filed a petition against the '633 Patent. The only entity to have done so is STMicro, *see* IPR2022-00252, but Wolfspeed and STMicro do not bear a "significant relationship" such that Factor 1 would favor discretionary denial. *Twitter v. Palo Alto Research Center Inc.*, IPR-2021-01398, Paper 12 at 40-41 (Mar. 15, 2022). Factors that inform whether two petitioners are related include their status as co-defendants in the same litigation; their shared interest in the same accused products; whether one petitioner has

attempted to join the other's proceeding; and whether there is evidence of coordination between the petitioners. *Id*. None of those factors are present here.

Purdue filed a complaint against STMicro on July 14, 2021, in the Western District of Texas, accusing products that are manufactured and sold by STMicro. Ex. 1017 at 1, 8-9. Purdue filed a separate complaint against Wolfspeed on October 28, 2021, in the Middle District of North Carolina, accusing products that are manufactured and sold by Wolfspeed and its predecessor Cree. Ex. 1016 at 1, 8-9. Accordingly, Wolfspeed and STMicro were sued months apart from one another and in different courts; they are not co-defendants; and they do not have overlapping accused products. Furthermore, Wolfspeed has not attempted to join the STMicro petition, and Wolfspeed and STMicro did not coordinate to prepare their petitions. The petitions present different grounds, and notably the STMicro petition does not rely on the Depetro or Choy references that are set forth in Grounds 1 and 2 of this Petition. In these circumstances, the Board has held that two petitioners challenging the same patent are not related and *General Plastic* Factor 1 weighs against discretionary denial. IPR-2021-01398, Paper 12 at 40-41.

Factor 2 is of "little probative value" here because Wolfspeed did not file the first petition and there is no significant relationship between Wolfspeed and STMicro. *Id*. at 41. Regarding Factor 3, the filing date of this Petition precedes both the preliminary response and institution decision in the STMicro proceeding.

See IPR2022-00252. Thus, Wolfspeed is not seeking to gain an unfair advantage by reviewing those documents before filing its Petition. This factor weighs against denial. *See* IPR-2021-01398, Paper 12 at 43.

Regarding Factors 4 and 5, Wolfspeed did not delay in filing this Petition. Purdue served its complaint on Wolfspeed on November 4, 2021. Between that date and the filing of this Petition, Wolfspeed undertook a diligent effort to analyze the '633 Patent, identify prior art, engage an expert, and prepare the Petition and accompanying exhibits. The timing of those efforts is reasonable, particularly because Wolfspeed filed its Petition before the preliminary response and institution decision in the STMicro proceeding. *See* IPR-2021-01398, Paper 12 at 42.[10] Furthermore, two of the three references in the Grounds of this Petition, Depetro and Choy, are not at issue in the STMicro proceeding. Thus, this is not a situation where Wolfspeed learned of those references from STMicro's petition and then unreasonably delayed in asserting them.[11] Accordingly, Factors 4 and 5 do not favor discretionary denial. *Id*. at 42.

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[10] Any delay between the filing of this petition and the STMicro petition is a consequence of Purdue's decision to sue Wolfspeed three-and-a-half months after STMicro. Ex. 1016, 1017.

[11] Wolfspeed was previously aware of the Ryu reference because it is assigned to Wolfspeed predecessor, Cree Inc. Ex. 1003. Wolfspeed did not delay in asserting Ryu, however, because Wolfspeed diligently prepared and filed its Petition within five months of Purdue serving its complaint.

Regarding Factors 6 and 7, joinder is not possible given the differences between the two Petitions, and, to the extent similarities exist, they will "provide some basis for efficiency" in the Board's resolution of the issues subject to review. *Id*. at 44. Accordingly, these factors weigh against discretionary denial.

On balance, the *General Plastic* factors weigh strongly against discretionary denial. The underlying rationale of *General Plastics* is to guard against abuse and strategic staggering of petitions and prior art assertions. IPR2016-01357, slip. op. at 17. This is not a case where Wolfspeed has attempted to abuse the IPR process or strategically stage the filing of its Petition relative to STMicro. Rather, it is a case where Purdue chose to sue Wolfspeed months after STMicro, and Wolfspeed worked diligently to prepare its Petition and file it in due course without any unfair advantage.

The *Fintiv* factors also weigh against discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (Mar. 20, 2020) (*precedential*). Regarding Factor 1, Wolfspeed intends to file a motion to stay the co-pending litigation upon institution of this Petition, if not earlier. Wolfspeed expects that the motion to stay would be successful given the litigation is still in the pleading stage, with no set procedural schedule or ongoing discovery.

Regarding Factors 2 and 3, the district court has not set a trial date, and the parties and court have invested minimal resources in the litigation. No discovery,

contentions, or claim constructions proceedings have taken place, and the district court has yet to rule on any motions.

Regarding Factor 4, it is unlikely there would be any conflict between the issues in this proceeding and the related litigation given the early stages of the litigation and the fact that Wolfspeed will be subject to estoppel under 35 U.S.C. § 315(e)(2).

Regarding Factor 6, the merits of the Petition are particularly strong given that the prior art relied upon was not before the Examiner during prosecution of the '633 Patent, Ryu teaches the SiC MOSFET features Purdue relied upon as a point of novelty during prosecution, and both Depetro and Choy teach the source region layout the Examiner found missing from the prior art.

B. 35 U.S.C. § 325(d)

Section 325(d) does not apply because the PTO has not previously considered the references Wolfspeed relies on in the proposed grounds, or any substantially similar references. First, neither Ryu nor any substantially similar reference was considered during prosecution. Ex. 1001 at 1-2. Indeed, the Applicant criticized the prior art advanced by the Examiner for its purported failure to teach the claimed JFET region in a silicon-carbide device—features that are present in Ryu. Second, the Examiner did not consider Depetro or Choy, or any other reference that teaches a plurality of base contact regions spaced apart in a

source region along a longitudinal axis. Ex. 1002 at 12-14. Indeed, the Examiner allowed the claims based on his determination that the prior art of record failed to disclose this feature. *Id*.

XIII. CONCLUSION

For the foregoing reasons, Wolfspeed requests that the Board institute *inter partes* review and cancel claims 9-11 of the '633 Patent.

Respectfully submitted,

Date: March 25, 2022

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CERTIFICATION UNDER 37 C.F.R. §42.24

Under the provisions of 37 C.F.R. §42.24, the undersigned hereby certifies that the word count for the foregoing Petition for *inter partes* review totals 13,839 words, not including the table of contents, table of authorities, mandatory notices, certificates, listing of exhibits, or listing of claims, as permitted under 37 C.F.R. § 42.24(a)(i).

Date: March 25, 2022

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e), 42.105(a), the undersigned hereby certifies service on the Patent Owner of a copy of this Petition, its respective exhibits, and Petitioner's Power of Attorney at the official correspondence address for the attorney of record for the '633 Patent as shown in USPTO PAIR via EXPRESS MAIL on March 25, 2022:

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Date: March 25, 2022

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